Ultra-thin Die Characterization for Stack-die Packaging

Wei Sun, W.H. Zhu, F.X. Che, C.K. Wang, Anthony Y.S. Sun and H.B. Tan
United Test & Assembly Center Ltd (UTAC)
Packaging Analysis & Design Center
5 Serangoon North Ave 5, Singapore, 554916
Email: Sun_Wei@sg.utacgroup.com, Tel: +65-65511345

Abstract

On both the process side and the reliability side, the mechanical strength of ultra-thin die is critical to ensure high assembly yield and good package reliability. To understand the mechanical strength and characteristics of ultra-thin die, comprehensive characterization work must be conducted. The current paper details the various ultra-thin die/wafer characterization and optimization work done by UTAC, where wafer is thinned down to 75μm and 50μm for stack-die application. At the wafer level, characterization tools like FSM's laser based system and Atomic Force Microscopy (AFM) were used to measure the finished wafer thickness, total thickness variation (TTV) and roughness. Two important dry polishing process parameters, namely applied load and stroke time, were investigated to understand their effects on those wafer characteristics. Subsequently, various types of dry polished wafers were diced into individual dies for die strength characterization study. Three test configurations, 3-point bending, 4-point bending and ring-on-ring, were used. Again, effect of dry polishing parameters on die strength was studied. Efforts were also paid to correlate die strength with wafer back surface roughness and finished wafer thickness.

1. Introduction

The trend towards miniaturized and high-density electronics calls for semiconductor packaging in the Z direction. Stack-die packaging is ideal due to its maturity and low cost of ownership as compared to other 3D packaging methods such as through-silicon-via and flip-chip-on-chip.

The stacking of multiple dies into a package is constrained by individual die thickness combined with the requirement for thin profile. Under the same package height, the thinner the die thickness is, the more the number of dies can be stacked. Therefore wafers are thinned down in order to increase the number of stacking dies. This brings some challenges. One is on the process side, where handling of thin wafer and pick-and-place of individual die are getting more and more difficult. For example, thinned die may not have enough mechanical strength to bear the force applied by pick-and-place process, where die cracking is not uncommon. For another example, the top die overhanging beyond the bottom die poises difficulty to wirebonding because the thin die may deflects too much to provide a stable platform for wirebonding. On the package reliability side, since multiple dies are stacked and silicon is known to be the major source of CTE mismatch within package, the thermo-mechanical stress is expected to impose higher load on thin die and thus may cause potential die-related failures.

Wafer backgrinding is widely adopted in thinning wafer thickness to required level. In those applications where wafers need to be thinned down to below 200μm, an added process called polishing is required to relieve the excessive residual stress and damages induced by backgrinding. This is to provide wafer with enough mechanical strength for subsequent assembly processes by minimizing those damages to wafer back surface. There are several wafer polishing approaches, namely dry polishing, chemical mechanical planarization, wet and dry etching, in the market. Their different features were discussed in detail in [1-2]. Because of the lower cost of ownership and environmental concern, only dry polishing is adopted here for thin wafer final polishing. However, several sets of dry polishing parameters and their impact on finished wafer thickness, TTV, roughness and die strength were evaluated.

The dry polishing process parameters under current investigation are applied load and stroke time because those are the most important parameters used to control the polishing process. In this study mirror wafers were thinned down to 75μm and 50μm. TTV of wafers were measured using FSM's laser based system. Surface roughness of polished back surface of mirror wafers was measured using both FSM's laser system and offline topometrix AFM. Also, roughness measurement was done on both 75μm and 50μm thinned wafers.

Die strength characterization was performed using 3-point bending, 4-point bending and ring-on-ring test apparatus. In 3-point bending test, the area of the highest stress contains mainly the die back surface and a minimal portion of the die edge. Thus die strength measured from this test is mainly attributed to the largest defect that is closest to the centerline of the specimen [3]. As for 4-point bending, the area of the highest stress contains both large portion of die edge and die back surface. Therefore, this method accounts for both die edge defects caused by wafer dicing and die back surface defects caused by wafer thinning [3-4]. In a ring-on-ring test setup, the die edges are not stressed. In this case, die strength measured accounts for only the defects on the die back surface [3-4]. In die strength characterization study, mirror wafers, RDL (redistribution layer) wafers and non-RDL wafers, were included. The difference for RDL wafer is that its die pads are redistributed through metal lines and dielectrics to desired locations other than their original locations for easy wirebonding, reduced wire length and wire sweep. Therefore, with the same thickness for RDL and non-RDL wafers, RDL wafer has thinner silicon thickness due to the existence of redistribution layer above silicon substrate. In the current study, the wafers used are all of 8-inch diameter.

2. TTV and Surface Roughness Characterization

In this part, the objective is to understand the effect of dry polishing parameters, namely applied load and stroke time, on

TTV and surface roughness of mirror wafers. 8-inch mirror wafers were dry polished to 75μm and 50μm. For subsequent thickness and TTV measurement using FSM's laser system, 60 points as shown in Figure 1 were measured on 75μm thick mirror wafers. A typical wafer thickness measurement contour is shown in Figure2.
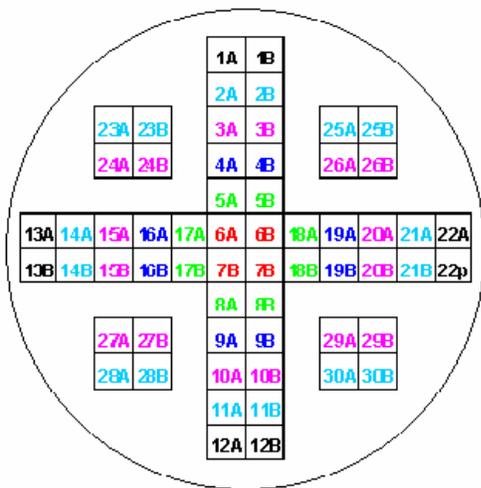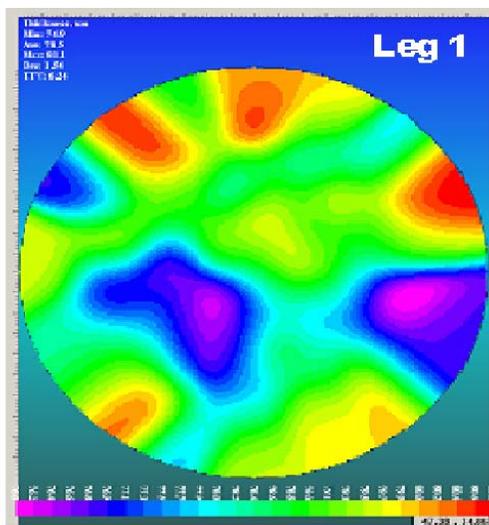

Figure 1: Measurement points across 8-inch wafer

Figure 2: Typical wafer thickness measurement contour using FSM laser system

TTV is the measurement of wafer planarity and is defined as the difference between the maximum and minimum values of the thickness of the wafer. Figure 3 shows the effect of dry polishing parameters on wafer TTV, standard deviation of thickness as well as average of measured thickness. It can be seen that TTV increases with more aggressive applied load and shorter stroke time during polishing process. In order to have minimal TTV longer stroke time and lower applied load are desirable. It is also observed that the standard deviation of wafer thickness follows the same trend as TTV. That is, longer stroke time and lower load gives smaller standard deviation.

Another important observation is that the finished wafer thickness differs with different set of dry polishing parameters. Because wafer thickness has a strong impact on die strength, such impact will be discussed later in die strength characterization section.
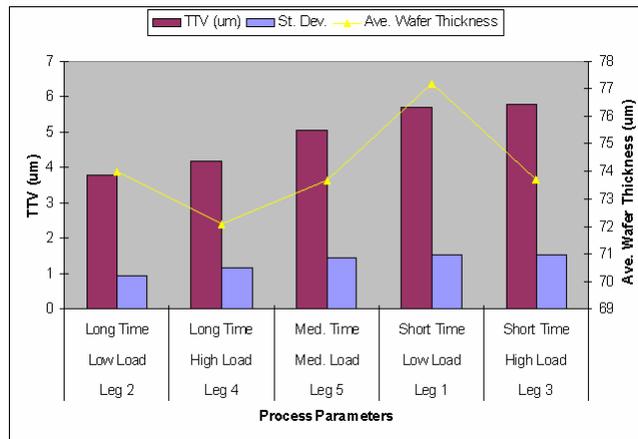

Figure 3: Effect of dry polishing parameter effects on finished wafer characteristics
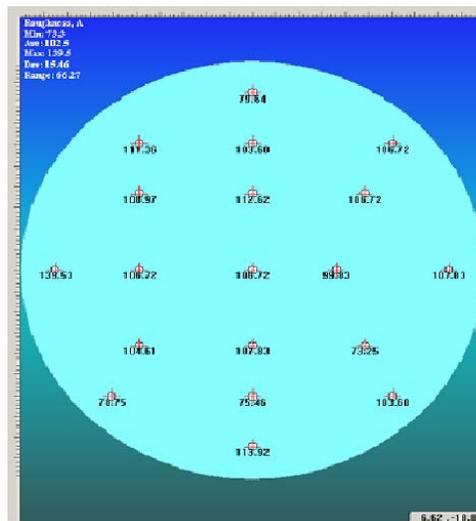

Figure 4: Illustration of typical 19 points roughness measurement using FSM laser system

FSM's laser system was also used to measure the roughness of polished wafer back surface. 19 points across the wafer as shown in Figure 4 were measured. The relationship between dry polishing parameters and averaged roughness values are plotted and shown in Figure 5 and 6. It is seen that for 75μm and 50μm, their trends between average roughness of polished surface and dry polishing parameters are completely different. While leg 1 (short stroke time and low applied load) gives best average surface roughness for 75μm wafer followed by leg 5, 4, 3, 2, this sequence is reversed for 50μm wafer. This probably means that if average roughness measured by FSM's laser system is considered as the evaluation target, different wafer thickness requires different optimal setting of dry polishing parameters.
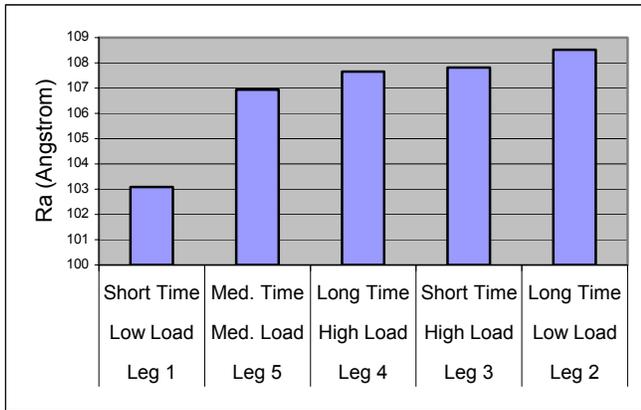
Figure 5: Effect of dry polishing parameter effects on finished wafer back surface average roughness (75μm thickness)
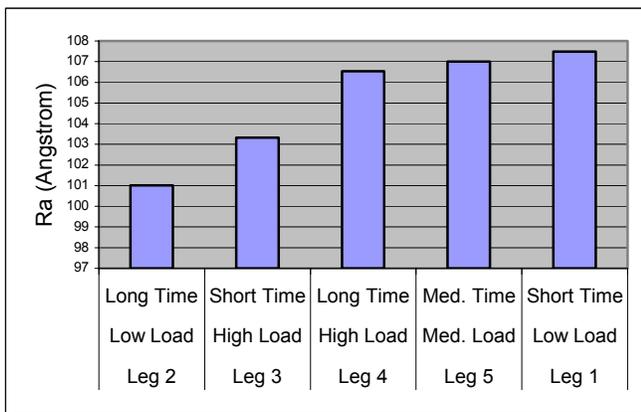

Figure 6: Effect of dry polishing parameter effects on finished wafer back surface average roughness (50μm thickness)
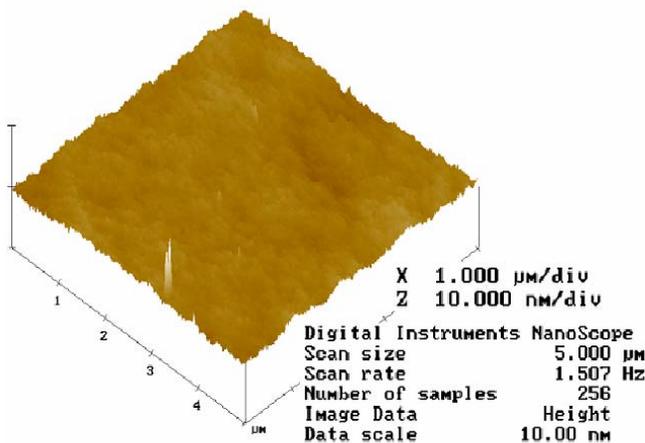

Figure 7: Typical surface morphology of under AFM for dry polished wafer

To make a comparison, surface roughness of dry polished mirror wafers was also measured using AFM. The center point of area 1A, 1B, 2A and 2B shown in Figure 1 was measured for both 50μm and 75μm wafers. A very localized area of 5x5μm was scanned. A typical AFM scanned contour is shown in Figure 7. The AFM roughness measurement results are shown in Table 1 and 2. As is shown, the localized surface roughness results for 50μm and 75μm still exhibit different trends against dry polishing parameters.

It should be noted that the roughness trends from FSM laser measurement and AFM measurement are quite different. The results from FSM machine are more for the overall back surface roughness at multiple selected points and are rather qualitative. In contrast, AFM scans a very localized area and accuracy is excellent. Comparing the two, AFM is more accurate in surface roughness measurement and should be seen as the preferred way. However, AFM scanning the whole wafer back surface may take prohibitively long time and generate overwhelming amount of data. Therefore, it is impossible to use AFM for the roughness measurement of the whole wafer back surface.

Table 1: Surface measurement values by AFM for 50μm polished wafer

	Ra values using AFM (Angstrom)				
Wafer	50um, Mirror wafer				
Leg #	Leg 1	Leg 2	Leg 3	Leg 4	Leg 5
Load	Low	Low	High	High	Medium
Time	Short	Long	Short	Long	Medium
Top	3.080	3.610	5.790	2.950	3.370
Bottom	3.560	3.150	6.340	3.250	4.520
Centre	3.630	4.330	4.610	3.350	3.560
Left	4.640	4.360	4.460	3.480	4.570
Right	5.410	3.800	5.060	3.700	3.730
Ave value	4.064	3.850	5.252	3.346	3.950
Rank value	4	2	5	1	3

Table 2: Surface measurement values by AFM for 75μm polished wafer

	Ra values using AFM (Angstrom)		
Wafer	75um, Mirror wafer		
Leg #	Leg 1	Leg 3	Leg 5
Load	Low	High	Medium
Time	Short	Short	Medium
Top	3.000	3.290	3.460
Bottom	3.050	4.230	3.790
Centre	2.960	3.470	4.260
Left	3.090	3.940	3.970
Right	3.250	2.980	4.090
Ave value	3.070	3.582	3.914
Rank value	1	2	3

3. Die Strength Characterization

Three different die strength characterization test configurations were used to measure the breaking load of die. They are 3-point bending, 4-piont bending and ring-on-ring tests. The schematic drawings and critical dimensions of different test setups are shown in Figure 8.

In this part, RDL and non-RDL wafers were tested by 3-point bending to study the effect of RDL layer on die strength and mirror wafers were tested by 4-point bending and ring-on-ring setups. An INSTRON Micro-force Tester was used to perform all the tests. Specially designed testing fixtures and loading heads were tooled up to hold the specimens and apply the loading.

Same as Section 2, the first objective of current work is to evaluate the effect of dry polishing parameters on die strength. Another objective is to study the wafer location dependence of die strength. It is known that wafer thinning

process will eventually leave some grinding marks on finished wafer back surface as shown in Figure 9. After thinned wafer is diced into individual dies, the pattern of grinding mark left on each individual die is different as shown in Figure 10. Those grinding marks or defects will have some impact on final die strength. However, because of the large of number dies on each wafer, current study was only able to evaluate the averaged die strength from wafer edge to wafer center. Therefore, dies picked from the location 1 to 22 as shown in Figure 1 were tested to study this location-dependence.
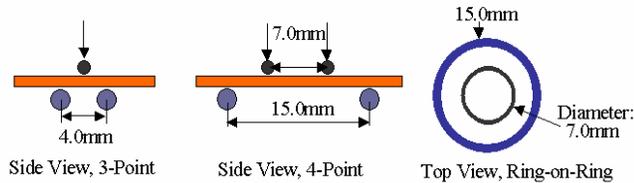
Figure 8: Schematic pictures of different test setup

Figure 9: Wafer thinning mark on backside of wafer
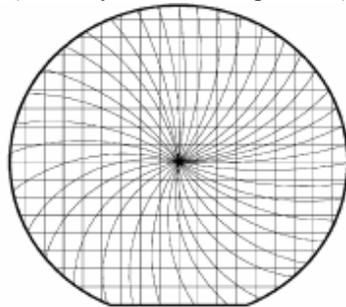(Courtesy of Disco Corporation)

Figure 10: Illustration of wafer thinning marks and die location

3-point bending

In a 3-point bending test, the die strength measured is mainly attributed to the largest and closest defect at the centerline of the specimen. For current test, both RDL and non-RDL wafers were used. Two thickness, 50μm and 75μm, were evaluated. The die size used is 9x5mm and testing configuration is shown in Figure 8. A typical force-extension curve obtained for 50μm RDL die is shown in Figure 11. It can be seen that the breaking load for 50μm RDL die is only around 0.18N and the loading curve exhibits the brittle nature of silicon material. The die strength along wafer diameter and effect of dry polishing parameters on die strength are shown in Figure 12 and 13 (refer to Table 2 for leg number and its corresponding dry polishing parameters).

It can be seen that with the same die thickness, non-RDL die has a much higher (more than 2-fold) breaking load than

RDL one especially for 75μm wafer. This is because at the same die thickness, non-RDL die has thicker silicon material than RDL die that contains redistribution layer above the silicon for re-routing of I/O pads. Such effect of redistribution layer on die strength can also be seen from the comparison of between breaking load of 75μm RDL die and that of 50μm non-RDL die. In this comparison, although the wafer thickness is different, both have comparable breaking load, showing the significance of redistribution layer. By comparing the breaking loads for 75μm and 50μm wafers it is also noted that the impact of RDL on die strength is decreasing with increased wafer thickness. Furthermore, it is also seen that 75μm die exhibits much higher (more than 2-fold) strength than 50μm die. Those die strength difference between RDL and non-RDL, 75μm and 50μm are important because this indicates that special care must be taken when handling and processing RDL and 50μm thin die because of its fragility.

From Figure 12, we can see that generally die strength at the wafer edge is higher than the inner part. In dry polishing process, it is known that the wafer edge portion has longer contact time with the dry polishing wheel. Therefore, the wafer edge portion is "more" polished and grinding defects are removed more effectively, making averaged die strength here higher.

As shown in Figure 13, for both RDL and non-RDL 75μm wafer, leg 1 provides the highest average die strength compared to the others. Percentage difference between best and worst leg is 78% and 22% for non-RDL and RDL wafer type respectively. This means that at 75μm, die strength of non-RDL wafer is more sensitive to dry polishing parameters. Also for 75μm wafer, other than a clear leg 1 with indication of highest die strength, the order of rank is not very consistent for different wafer type. From best to worst:

Non-RDL: Leg 1>Leg 4>Leg 3>Leg 2
RDL: Leg 1>Leg 2>Leg 3>Leg 4

However, for 50μm wafer, there is no consistent ranking of performance for RDL and non-RDL wafer type. Percentage difference between best and worst leg is 30% and 25% for non-RDL and RDL wafer type respectively

Non-RDL: Leg 3>Leg 1>Leg 2>Leg 4
RDL: Leg 2>Leg 3>Leg 1>Leg 4

It should be noted that die strength is a combined effect of die thickness, back surface roughness and die edge defects. In the context of 3-point bending, die thickness and roughness are the decisive factors. From Figure 3 we can see that leg 1 gives highest finished wafer thickness. Furthermore, both overall and local roughness measurement for 75μm wafer show that leg 1 give the lowest surface roughness. So those two advantages give leg 1 the highest die strength among all legs for 75μm wafer. For 50μm wafer, it is difficult to determine which factor, thickness or roughness, plays a more important role in affecting die strength. Therefore, the best leg for 50μm RDL and non-RDL is not the same and ranking of legs is not consistent.
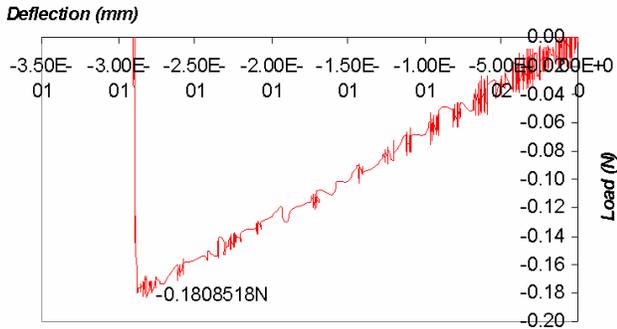
Figure 11: Force-extension curve for 50μm RDL die

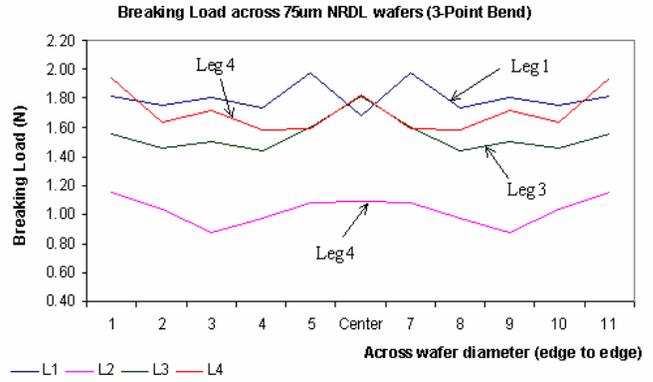

Figure 12: Die strength along wafer diameter and effect of dry polishing parameters
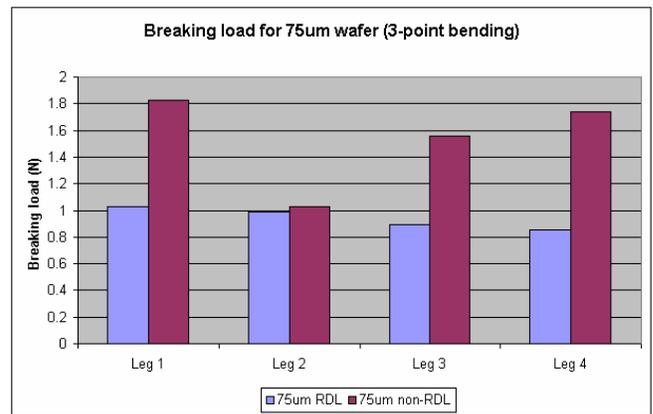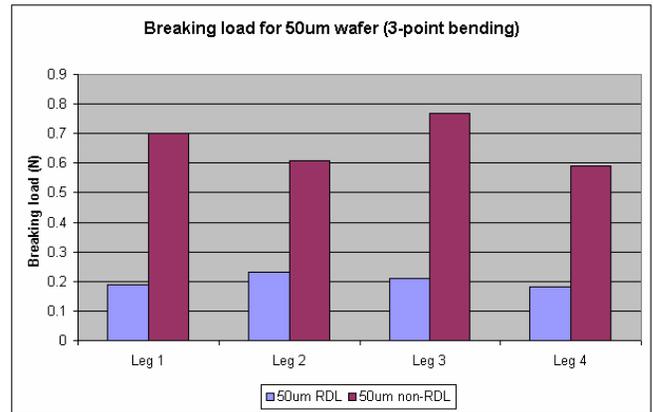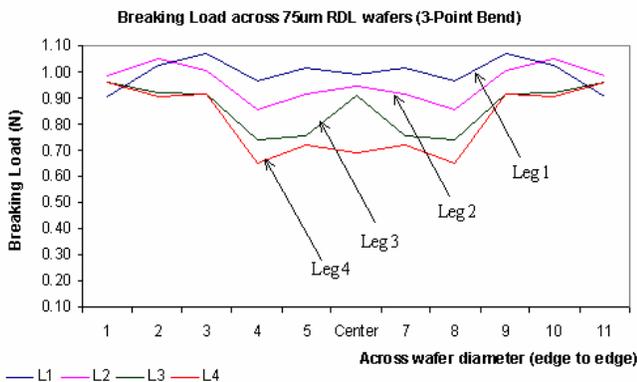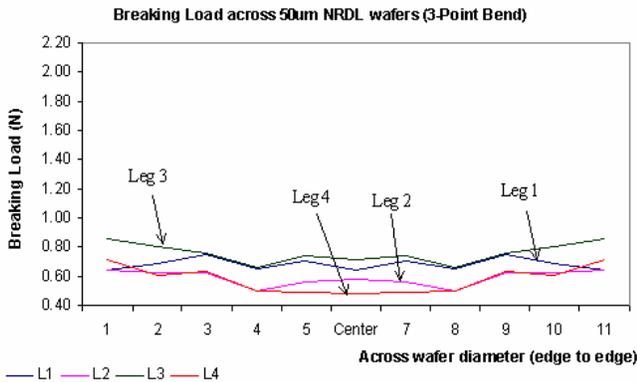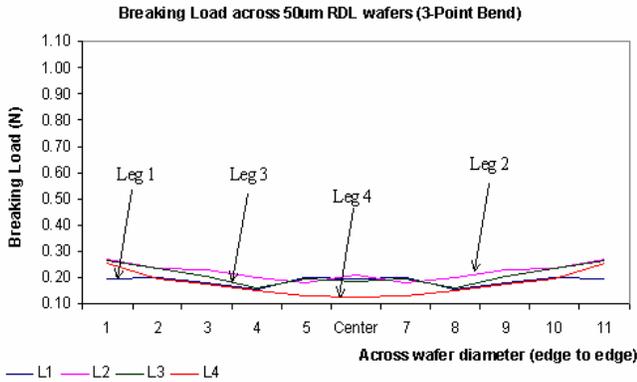

Figure 13: Die strength (3-point bending) comparison among different legs

4-point bending

Die strength test using 4-point bending accounts for both die edge and die back surface defects in the portion between the two supporting spins. As per discussion in 3-point bending section, die thickness, back surface roughness and edge defects caused by singulation are the factors that affect the final die strength. Therefore all of those three factors will come into play in 4-point bending. In this part, mirror wafers of 50μm and 75μm were used for current test. The singulated

die size is 20x5.5mm and test configuration is shown in Figure 8.

We can see from Figure 14 that for 75μm wafer, same as in 3-point bending test leg 1 still provides the highest die strength compared to the others. This could still be due to the highest thickness and lowest roughness of leg 1 wafer.

For 50μm thick wafer, leg 1 also provides the highest die strength compared to other legs. Percentage difference between best and worst legs is 20%.

The rank of die strength of different legs for both 75μm and 50μm wafers is as follows:

75μm mirror wafer: Leg 1>Leg 3=Leg 4>Leg 2>Leg 5
50μm mirror wafer: Leg 1>Leg 3=Leg 2=Leg 5>Leg 4

As die strength is the combined effect of die thickness, back surface roughness and edge defects, it is difficult to determine which factor is more important than others. Therefore the ranking of legs for 75μm and 50μm is not the same.
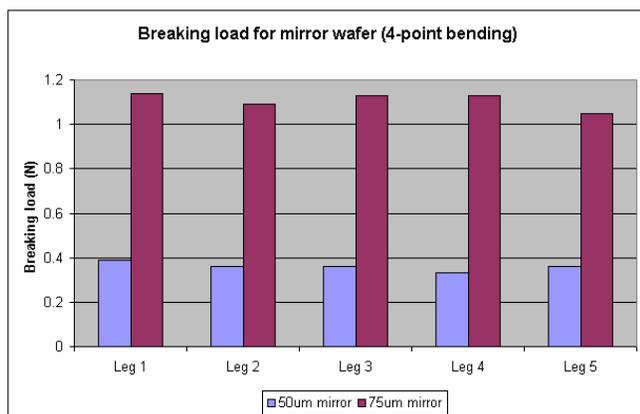

Figure 14: Die strength (4-point bending) comparison among different legs

Ring-on-ring test

In a ring-on-ring test setup, the measured die strength accounts for only the defects on the die back surface within the top ring diameter area. Therefore, only die thickness and back surface roughness will come into play. In the current study, the die size used is 20x20mm and same as in 4-point bending only mirror wafers dry polished to 50μm and 75μm were used for the test.

It is seen from Figure 15 that for 75μm thick wafer, leg 1 again provides the highest die strength compared to others. Furthermore, the ranking of legs for ring-on-ring test of 75μm wafer is the same as the ranking in 4-point bending except that in the current case leg 3 generates higher die strength than leg 4 while in 4-point bending leg 3 gives same die strength as leg4. This probably means in 4 point bending, the die edge defect also played important role in affecting die strength.

For 50μm thick wafer, leg 2 provides the highest die strength compared to other legs. Same as the discussion in 3-point and 4-point bending, it is difficult to determine which factor is more important than others in determining die

strength. Therefore the ranking of legs for 75μm and 50μm is not consistent.

The rank of die strength of different legs for both 75μm and 50μm wafers is as follows:

75μm mirror wafer: Leg 1>Leg 3>Leg 4>Leg 2>Leg 5
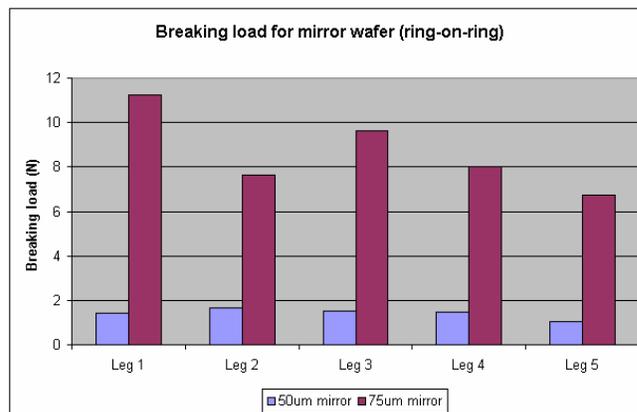50μm mirror wafer: Leg 2>Leg 1>Leg 4>Leg 3>Leg 5

Figure 15: Die strength (ring-on-ring) comparison among different legs

Summary and Conclusions

Various characterizations were done to study the effects of dry polishing parameters on finished wafer thickness, back surface roughness, TTV and die strength. The following summary and conclusions can be obtained.

(1) It can be observed that TTV increases with more aggressive applied load and shorter stroke time. In order to have minimal TTV longer stroke time and lower applied load are desirable.

(2) Finished wafer thickness differs with different set of dry polishing parameters and such difference in finished thickness has significantly impact on die strength especially for 75μm wafer.

(3) Polished wafer back surface roughness was measured using both FSM's laser system and AFM machine. It is found that this two measurement methods give different rankings of dry polishing parameters for both 75μm and 50μm wafers. However, for 75μm wafer, leg 1 dry polishing parameter was consistently found to generate the minimal wafer back surface roughness.

(4) The measurement by FSM's laser system is qualitative and more for the averaged overall roughness of back surface. In contrast, measurement done by AFM is accurate and very localized. Therefore, this indicates that a tool combining the advantages of the two is needed for accurate and quick measurement in order to accurately assess the quality of polished wafer back surface.

(5) It is found that the breaking load of 75μm die is significantly higher (more than 2-fold) than 50μm die. Besides, the existence of RDL layer has a great impact on die strength. Such impact can be seen from the founding that 75μm RDL die even has comparable die strength with 50μm non-RDL die.

(6) Die strength at the wafer edge is higher than the inner part. This is mostly because wafer edge portion has longer contact time with the dry polishing wheel during polishing process. Therefore, the wafer edge portion is "more" polished and grinding defects are removed more effectively, making averaged die strength here higher.

(7) In the 3-point bending and ring-on-ring tests, die thickness and roughness are the decisive factors. That's why leg 1 with highest thickness and lowest roughness gives highest die strength among all legs for 75μm wafer. For 50μm wafer, it is difficult to determine which factor, thickness or roughness, plays a more important role in affecting die strength. Therefore, the best leg for 50μm wafers is not the same and ranking of legs is not consistent.

(8) In the 4-point bending test, die strength is a combined effect of die thickness, back surface roughness and die edge defects. However, it seems die edge defect did not play a very important role and this is why the ranking of legs for 75μm wafer remains the same as ring-on-ring test. Again, for 50μm wafer, it is difficult to determine which factor, thickness or roughness or die edge defect plays a more important role in affecting die strength. Therefore, the best leg for 50μm wafers is not the same and ranking of legs is not consistent.

References

1. Larry Wu, Jacky Chan and C.S. Hsiao, "Cost-Performance Wafer Thinning Technology", *Proceedings of ECTC2003*, pp. 1463-1467.
2. Werner Kroninger and Franco Mariani, "Thinning and Singulation of Silicon: Root Causes of the Damage in Thin Chips", *Proceedings of ECTC2006,* pp. 1317-1322.
3. Betty Yeung and Tien-Yu Tom Lee, "An Overview of Experimental Methodologies and Their Applications for Die Strength Measurement", IEEE Trans. On Components and Packaging Tech., Vol. 26, No. 2, June 2003, pp. 423-428
4. B. Cotterell, Z. Chen, J.B. Han and N.X. Tan, "The Strength of the Silicon Die in Flip-chip Assemblies", Journal of Electronic Packaging., Vol. 125, March 2003, pp. 114-119
.