Thermal Evaluation of Two Die Stacked FBGA Packages

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Abstract

This paper presents the thermal evaluation of two die stacked FBGA (D2-FBGA) with identical die structure. Thermal performance was evaluated experimentally with the package size of 15mmx15mmx1.2mm, 2 signal metal layers, 208 ball count containing an identical die stack configuration with two Delco PST4-02 thermal test dies of 6.35mmx6.35mm size each. Experiments were carried out using JEDEC still air chamber as per JESD 51.2 [10], JEDEC specified forced air environmental condition as per JESD 51.6 [11] with 1m/s & 2m/s and ring cold plate for theta JB measurement as per JESD 51.8 [7]. Junction temperature was measured by Electrical Test Method (ETM) as outlined by JEDEC standard JESD 51.1 [8]. Board and ambient temperatures were measured by thermocouples. Experimental data were obtained for 1S0P and 1S2P PCB with a sample size of five to calculate the temperature rise above the ambient for both top and bottom dies in still and forced air JEDEC environmental conditions. The same data were used to generate the thermal resistance matrix for linear super position matrix formulation to identify the changes in thermal cross talk between the dies at various power level combinations [1].

The commercially available Flotherm V6.1 software code was used to create and simulate CFD model of D2-FBGA package in JEDEC specified still air, forced air ring cold plate set-up for theta JB. The model was simulated for various power level combinations and validated successfully within the agreeable limit of accuracy (10 %) against experimental results for the temperature rise, Psi JB (ψ_{jb}) in theta JA (θ_{ja}) condition with 1S0P and 1S2P boards and theta JB with 1S2P board.

Keywords:

D2-FBGA, thermal evaluation, CFD modeling and simulation, thermal testing and results validation

Nomenclature:

θ_{ja}/R_{ja}-Die junction to ambient thermal resistance, $^oC/W$
θ_{jb}/R_{jb}-Die junction to board thermal resistance, $^oC/W$
θ_{jc}/R_{jc}-Die junction to case thermal resistance, $^oC/W$
ψ_{jb} & ψ_{jt} – Thermal characterization parameters, $^oC/W$
Q- Power dissipation, W
∇T-Temperature rise above the reference or ambient, ^oC
LSP-Linear Super Position
PCB-Printed Circuit Board
TSP-Temperature Sensitive Parameter

1. Introduction

BGA packaging solution is known for higher I/O counts. Moreover, chip stacking in BGA is becoming a need for memory packages and other applications due to the demand for compactness and additional functionalities. 3-D chip stacking is the main acceleration for Moore's law due to the density of IC elements on the package surface area is multiplied by the number of stacked layers. In stacked die packages, volumetric heat density increases with increase in number of die. As more than one heat source is present in the stacked packages, thermal evaluation and presenting the thermal data are different from single die or single heat source IC packages. For single die packages, thermal characterization is straightforward and the methodology is also addressed by the industry standard JEDEC. Thermal characterization of stacked die packages is complicated. Because thermal resistance θ_{ja} can not be easily defined for multi die pacakges [1]. UTAC (United Test and Assembly Center Ltd) makes varieties of single die and multi-die BGA packages with excellent electrical, mechanical and thermal performance. As it is challenging to evaluate the multi-die packages thermally, a simple die stacking, two die stacked FBGA (D2-FBGA) package with identical die structure was chosen to demonstrate the thermal evalution methodology.

Normally thermal performance of the package is measured in terms of its temperature differernce between the junction temperature of the chip and reference temperature divided by the known power dissipated. This is denoted R_{jx} or θ_{jx} [1]. Here, the reference temperature can be either the ambient temperature for θ_{ja} or θ_{jma}, the package case temperature for θ_{jc} or the borad temperature close proximity to the package case for θ_{jb}. In θ_{jc} and θ_{jb} condition, almost the entire power will be dissipated through the specified reference point surface area. When we find the case and board temperature during θ_{ja} or θ_{jma} environmental conditions and this can be used to compute thermal characterization parameters ψ_{jt} and ψ_{jb}. Even though we use total power to get ψ_{jt} and ψ_{jb}, the entire power is not dissipated through case or board.

As stacked die packages have several heat dissipating devices residing within the same package, we do not use θ_{ja}, which assumes one reference junction, one heat source, and does not account for thermal crosstalk between the dies. There is no industrial standard for stacked die package thermal characterization till now. For identical die stacked structure and power dissipation, Bar-Cohen's [12] approach of lumping the device together holds reasonable accuracy in predicting the thermal behaviors. But a few literatures are suggesting to use linear super position principle to specify thermal resistance matrix with accommodationg non-linear multiplier in the evalutation of temperature rise in all the dies [1]. This helps to estimate the temperature rise and thermal cross talk between the dies for the other power levels or power split.

2. Construction of D2-FBGA and its details

Fig. 1 illustrates the die stack configuration of D2-FBGA. This has 2 metal layers with 15mmx15mm substrate about 0.2mm thickness and 208 ball count with depopulated array of solder ball and 0.8 mm pitch as shown in Fig. 2.

Fig 1. D2-FBGA structure

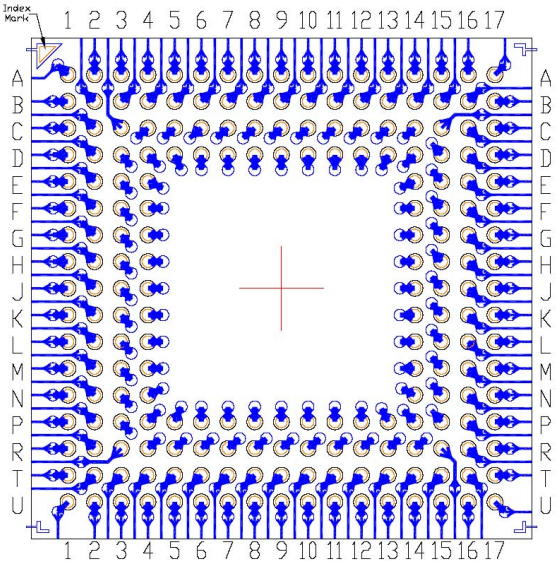


Fig 2. M2-Layer of substrate

The overmold thickness was 0.7mm with the same size of substrate. Two Delco PST-4 (6.35mmx6.35mm) thermal dies which meet the thermal requirements specified by the JEDEC specification EIA-JESD 51-4 [5] were stacked to form an identical structure in FBGA. Both the dies were background to 0.14mm thickness and the bottom die is attached with the substrate by a die attach material. Bottom and top die were stacked together by a spacer adhesive of 0.15mm thickness as shown in Fig 1. Spacer adhesive thickness was sufficient to accommodate wirebond loop height. Substrate has top and bottom solder mask of 0.025mm thickness. Top and bottom metal layers (Cu foil+Cu plating) of 0.022 mm thickness. No thermal via is present in the substrate.

3. Thermal test board details

The sample size was five for each 1S0P and 1S2P PCB. First 5 samples were undergone for surface mounting to a 101.5~114.5~1.60mm 1S0P thermal test PCB and another five samples were surface mounted with 101.5~114.5~1.60mm 1S2P thermal test PCB. The test PCB stackup consists of top and bottom solder mask layers of 0.035mm thick, top and bottom trace layers of 0.070mm thick, power and ground plane of 0.035 mm thick. PCB did not contain any thermal via. D2-FBGA with 2 Layer and 4 Layer PCB are shown in Fig 3.

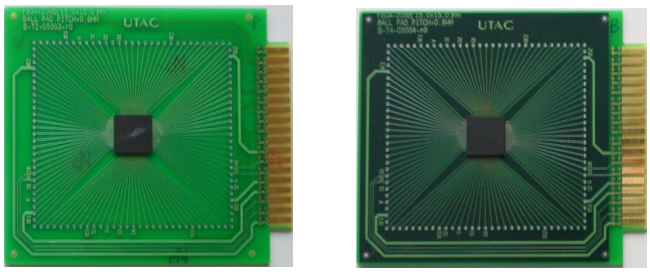


Fig 3. 2L & 4L PCB with D2-FBGA

4. Description of test vehicle and procedure

Table 1 shows the typical power dissipation matrix, which was chosen for experimental thermal evaluation of D2-FBGA. First two rows of matrix are for forming the thermal resistance matrix [2]. For the convenience total power was chosen as 1W in all the cases. Last three rows of matrix were to study the feasibility of using LSP.

Table 1 Power dissipation Matrix

	S.No:	Stacked Die Thermal Experimental Power Dissipaion Matrix, W					
		Still Air		Forced Air			
				1m/s		2m/s	
		Top Die	Bottom Die	Top Die	Bottom Die	Top Die	Bottom Die
To Form Thermal Resistance Matrix	1	1	0	1	0	1	0
	2	0	1	0	1	0	1
To Check LSP Method	3	0.25	0.75	0.25	0.75	0.25	0.75
	4	0.5	0.5	0.5	0.5	0.5	0.5
	5	0.75	0.25	0.75	0.25	0.75	0.25

One cubic foot still air chamber per JEDEC standard JESD51-2 [10] was used to perform natural convection thermal testing to find ∇T and ψ_{jb} under still air chamber as shown in the Fig 4. To find ∇T and ψ_{jb} in forced air convection 1m/s and 2m/s, wind tunnel was used. Fig 5 shows the test section set-up of the forced air convection environment, which is a part of wind tunnel. For all the above experimental cases, the ambient temperature was kept about 21~23 °C. In order to obtain θ_{jb}, ring cold plates were used as per JESD 51-8 [7] with appropriate water flow rate. The experimental set-up is shown in Fig 6.

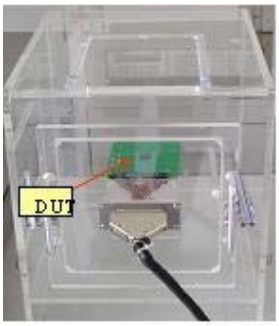


Fig 4: Still air chamber

Fig 5: Forced air section

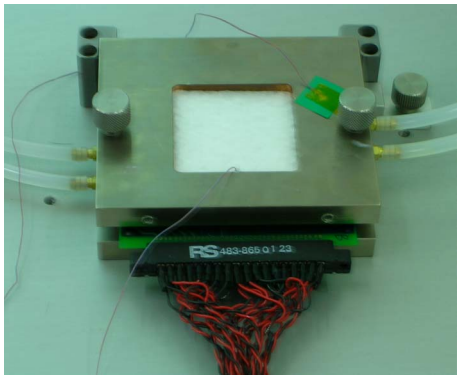


Fig 6. Ring cold plate set-up for θ_{jb}

In order to reduce the contact resistance, appropriate pressure was given to establish a better contact between ring cold plates and PCB. As per JEDEC guidelines, an insulation was given on the PCB board to avoid the trace break and merger of traces due to the pressure. For θ_{jb} experiments, 4L board was used to enable the heat to flow to ring cold plate efficiently as per standard. For each test, θ_{jb} was calculated by the difference between maximum junction temperature and board temperature divided by the power dissipated. θ_{jb} was computed for the test conditions when top die dissipated 1W, bottom die dissipated1W and each die dissipated 0.5W.

During the measurements, a 'T' type 36 gauge thermocouple was attached on the trace of the PCB in 1mm away from the package edge to calculate ψ_{jb} and θ_{jb}. One more 'T' type 36 gauge thermocouple was used to measure the reference temperature (ambient or cold plate temperature). As per JESD 51-1 [8], junction temperature was measured by standard Electrical Test Method (ETM). Before actual measurement was carried out, each PST-4 thermal test die was subjected to standard K factor calibration against Memmert ULP 400, a precision programmable heating oven or thermal chamber. All calibration and measurement were performed using single diode. Obtained K factor was used in the test program to generate the temperature rise Vs time profile automatically upon specified power level. A PCB edge connector was used to communicate with the package and all other items like DC power supply, Keithley switching mainframe and Keithley source meter. All measuring instruments were interconnected with GPIB interface and measurement parameters were controlled and monitored by a custom made JEDEC compliant software. Thermal evaluation was conducted according to the matrix defined by Table 2. For each thermal test, power was applied to the thermal test die and the steady state temperatures were captured when PCB and package case were thermally stablized. The transient data were also collected and the stabilized stage values were taken for verification and calculation. A thermal test sample size of 5 was used for each testing configuration and the mean value was found and compared with the prediction made by CFD simulation. For the table 2, θ_{ja} or θ_{jb} refers to difference between the "Maximum junction temperature and reference temperature" for the unit power application.

Table 2 Thermal evaluation matrix

Test conditions with 0, 1 and 2 m/s wind speed		
PCB	D2-FBGA (Identical Die)	
	θ_{ja}	θ_{jb}
1s0p	x	NA
1s2p	x	x

5. CFD modeling

FLOTHERM®[12], a leading Computational Fluid Dynamics (CFD) software code specially developed for the electronics industry, was employed to predict the package thermal performance for each test condition. Fig. 7 depicts the solid model of D2-FBGA.

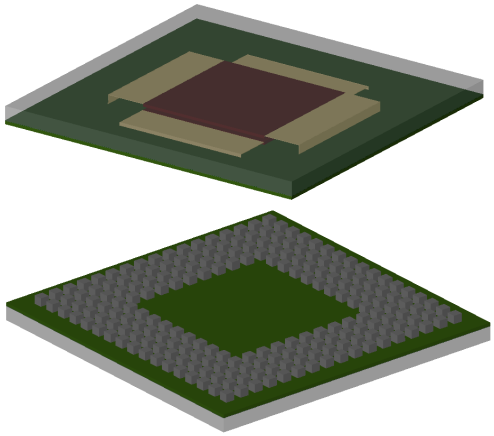


Fig 7. Flotherm solid model: Top and Bottom View

D2-FBGA package is accurately modeled in detail in the CFD software to capture the actual thermal behavior of exact physical structure. Here substrate and PCB traces are not modeled in detail. Instead, it is modeled as volume averaged layer with appropriate thermal conductivity. Wire bonds are modeled as equivalent thermal conductivity embedded solid cuboid with orthotropic thermal property. All other package interior and exterior parts were represented as a series of embedded conductive solid cuboidal blocks with isotropic thermal conductivities. Radiation was applied to all the exposed surfaces, whose emissivity was assumed to be 0.8. Material thermal conductivities used are listed in the Table 3.

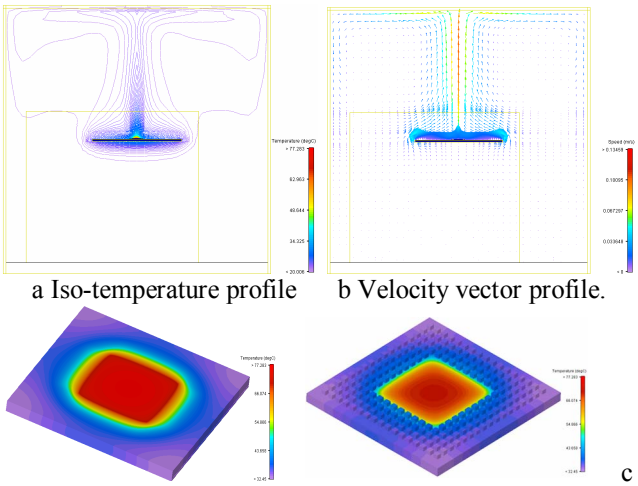
Table 3. Material Properties

S/n	Material	K (W/mK)
1	Mold compound	0.8
2	Die to substrate attach	0.3
3	Spacer adhesive	0.3
4	PCB trace	390
5	Solder	50.9
6	Die	Temp. dependent*
7	Bond wire	296

*K(Si)=117.5-0.42 (T-100)

Localized grid was used to capture temperature profile and flow pattern in the areas of interest or where rapid changes are expected. Grid-dependent solution studies were performed by adjusting grid size. It is assumed that a converged result has been achieved if the junction temperature is changed by less than 1% with a finer gridding.

Laminar and turbulent flow were assumed for natural and forced convection respectively with ambient temperature of 20°C. Fig. 8 shows the temperature profile for D2-FBGA with 4L PCB at natural convection when top die dissipating 1W. Both still and forced air simulations were subjected to conjugate heat transfer mode.



a Iso-temperature profile b Velocity vector profile.

c Surface temperature profile of D2-FBGA

Fig 8. Still air simulation results of D2FBGA (4L)

Thermal simulation was performed for the cases as specified in the Table 1 and Table 2 with appropriate JEDEC specified test environmental conditions. Simulation results are presented under the results and discussion section. Ring cold plate set-up was modeled appropriately and the results were captured for the cases in the Table 5. As conduction was the predominant heat transfer in ring cold plate simulation, conduction alone was modeled and solved. Fluid temperature was assumed to be 23 °C. The typical side and top view of Flotherm wire frame model is shown in the Fig 9.

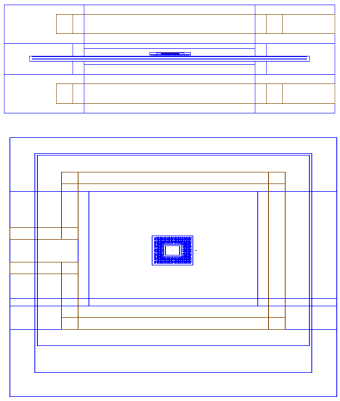


Fig 9. D2-FBGA with Ring Cold Plate

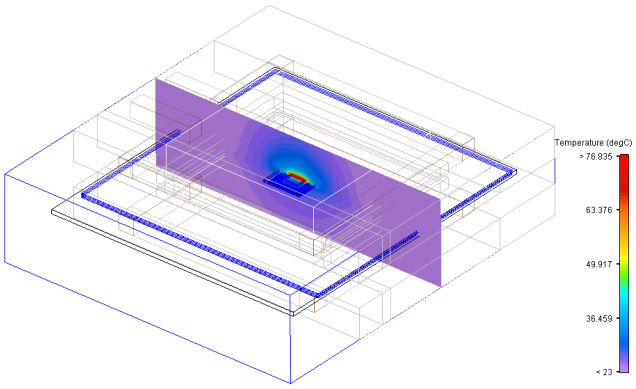


Fig 10. Temperature profile of θjb test

2-D temperature profile of D2FBGA (4L) is shown in Fig 10. This is for the case when top die dissipated 1W power.

5. Results validation and discussion

For the sample size of five in each experimental test, the mean thermal performance was found. Moreover, standard deviation was found to be less than 1°C. As mentioned, temperature rise ∇T was calculated for stacked die packages rather than θ_{ja}. Thermal performance comparisons are shown in the Table 3 and Table 4 for 1S0P and 1S2P boards respectively. In general, 10% of error between measurement and simulation is accepted. For D2-FBGA, error is less than 10% in all the cases.

The experimental results are plotted against the simulated (predicted) results and shown the trend to know how the bottom and top die behaved when the power was applied to the dies separately with 1W.

Thermal performance of D2-FBGA with 1S0P board when top die was activated with 1W is shown in Fig 11. The trend is similar between experiments and simulation. The temperature difference between top and bottom die is consistant in all the testing conditions due to spacer adhesive (thickness and its thermal conductivity).

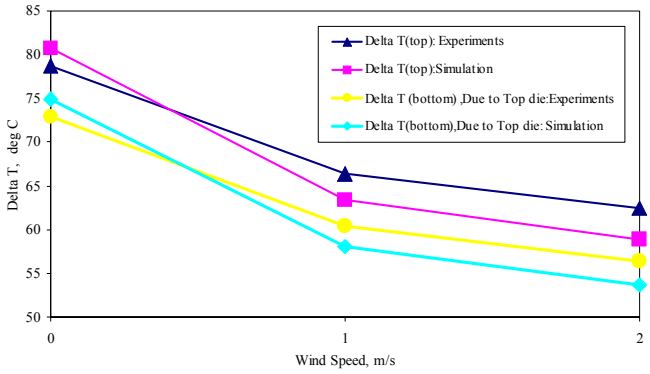


Fig 11. D2-FBGA with 1S0P when top die at 1W

Thermal performance of D2-FBGA with 1S0P board when bottom die was activated with 1W is shown Fig 12. The trend is similar between experiments and simulation. When bottom die dissipates power, temperature rise is lesser due to easier heat conduction path to PCB rather than top die.

Table 3: D2-FBGA with 1S0P: Validation

		Condition	Delta T (top)			Delta T (bottom)			Psi-jb		
			Experiments	Simulation	% Error	Experiments	Simulation	% Error	Experiments	Simulation	% Error
Still		Top Die@ 1W	78.76	80.70	-2.46	72.85	74.94	-2.87	51.81	51.14	1.29
		Bottom Die @1W	72.52	74.86	-2.76	78.15	77.93	0.28	52.43	51.14	2.45
Forced	1m/s	Top Die@ 1W	66.34	63.44	4.37	60.43	58.11	3.84	42.62	43.68	-2.49
		Bottom Die @1W	60.26	57.92	4.15	65.77	61.33	6.75	42.94	41.46	3.45
	2m/s	Top Die@ 1W	62.40	58.91	5.59	56.43	53.73	4.78	40.74	41.88	-2.79
		Bottom Die @1W	56.25	53.01	6.06	61.53	56.55	4.76	41.27	39.81	3.55

Table 4: D2-FBGA with 1S2P: Validation

		Condition	Delta T (bottom)			Delta T (top)			Psi-jb		
			Experiments	Simulation	% Error	Experiments	Simulation	% Error	Experiments	Simulation	% Error
Still		Top Die 1W	50.18	51.47	-2.58	55.39	57.28	-3.41	41.39	44.77	-8.18
		Bottom Die 1W	55.10	54.25	2.06	50.16	51.34	-2.34	41.12	41.70	-1.41
Forced	1m/s	Top Die 1W	45.78	43.96	3.97	50.84	49.43	2.77	39.29	41.37	-5.29
		Bottom Die 1W	50.58	46.97	7.61	45.54	43.78	3.86	39.34	38.88	1.16
	2m/s	Top Die 1W	43.81	41.70	4.81	48.81	47.04	3.63	38.31	40.03	-4.48
		Bottom Die 1W	49.06	44.82	8.17	43.98	41.50	5.64	35.36	37.78	-6.85

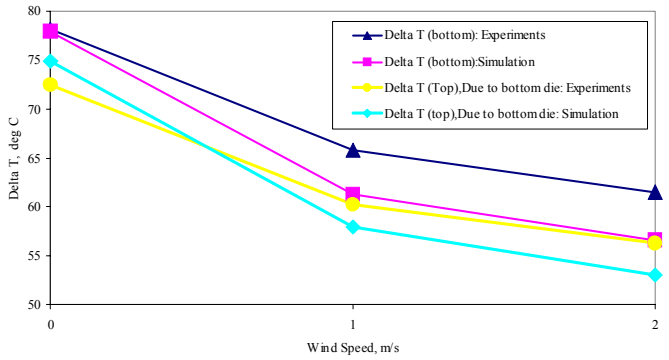


Fig 12. D2-FBGA with 1S0P when bottom die at 1W

Again the trend for D2-FBGA with 1S2P board is also simlar to 1S0P board and shown in Fig 13 and Fig 14.

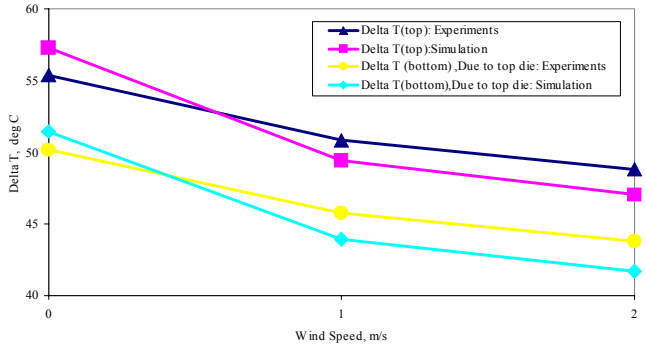


Fig 13. D2-FBGA with 1S2P when top die at 1W

It is suspected that the errors between experiments and simulation are due to lack of detail modeling of traces, slight variation in the geometric details with physical structure and temperature related non-linearity's in the material properties. The temperature difference between top and bottom die is slightly different in simulation and experiments. This may be due to the variation of spacer adhesive thickness and size in x-y direction with actual prototype.

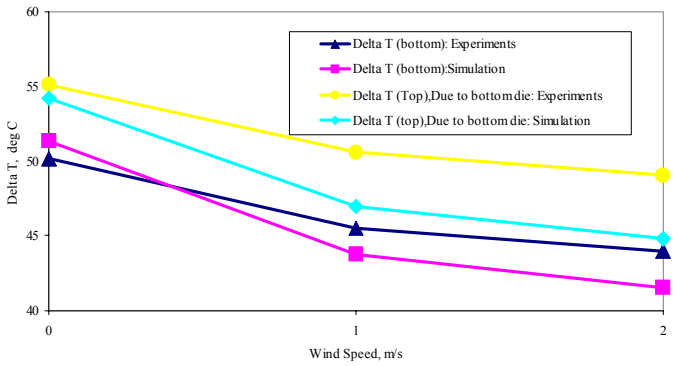


Fig 14. D2-FBGA with 1S2P when bottom die at 1W

D2-FBGA was subjected to θ_{jb} environment [7] for measurement and simulation to know its thermal performance. θ_{jb} was calculated based on the maximum temperature rise divided by the total power for all the cases. The mean thermal performances were found in each test of experiments with the sample size of five. Moreover, it was found that the standard deviation is less than 1°C. Thermal performance comparion is shown in the Table 5.

Table 5: Theta JB results of D2-FBGA

	Theta JB, C/W		
	Experiments	Simulation	% Error
Top die @ 1W	42.4	45.3	-6.9
Bottom die @ 1W	40.8	42.8	-4.9
Both die @ 0.5W	40.0	41.8	-4.5

Experimental thermal evaluation is difficult and tedious for multi-die IC packages as it requires more sourcing channels to pump the power to all the dies, simultaneous sensing channels to sense back all the die temperatures and measurement parameters. But in numerical modeling, there is

no difficulty in evaluating the multi-die packages [2]. Here, an attempt is made to demonstrate the LSP method in evaluating D2-FBGA thermally. First step of evaluation is to formulate the thermal resistance matrix. For that, it is required to get thermal resistances for top and bottom die of D2-FBGA when top and bottom die was activated separately with the known power. This was obtained as follows.

When top die (Die 1) was activated,

$$R11 = (\nabla T11/Q1) \;\&\; R21 = (\nabla T21/Q1). \quad (1)$$

When bottom die (Die 2) was activated,

$$R22 = (\nabla T22/Q2);\; R12 = (\nabla T12/Q2). \quad (2)$$

If the package having "N" heat sources, the thermal resistance matrix will be N-by-N matrix, [R]. The heat dissipation of each die is formed into a column matrix, [Q]. The difference between the die temperature and ambient temperature also forms a column matrix, [∇T], with ∇T1 and ∇T2 where ∇T1 equals to junction temperature of the top die minus ambient temperature and ∇T2 equals to junction temperature of bottom die minus ambient temperature. Using determined thermal resistance matrix, top and bottom die temperatures can be evaluated for various power levels based on the principle of super position.

General reporting format of thermal resistance matrix [1] is

$$\begin{bmatrix} R11 & R12 \\ R21 & R22 \end{bmatrix}$$

For D2-FBGA with 1S0P board, experimental thermal resistance matrix for still air,

$$\begin{bmatrix} 78.76 & 72.52 \\ 72.85 & 78.15 \end{bmatrix}$$

for 1m/s forced air,

$$\begin{bmatrix} 66.34 & 60.26 \\ 60.43 & 65.77 \end{bmatrix}$$

and for 2m/s forced air

$$\begin{bmatrix} 62.4 & 56.25 \\ 56.43 & 61.53 \end{bmatrix}$$

These matrixes can be used to evaluate the thermal performance of top and bottom die for various power levels and to study the thermal cross talk between them. For example, if we want to find out the thermal performance of D2-FBGA in still air condition when top die dissipates 0.25W and bottom die dissipates 0.75W. The formulation will be as follows:

$$\begin{bmatrix} R11 & R12 \\ R21 & R22 \end{bmatrix} * \begin{bmatrix} Q(top) \\ Q(bot) \end{bmatrix} = \begin{bmatrix} Delta\ T(top) \\ Delta\ T(bot) \end{bmatrix}$$

Hence,

$$\begin{bmatrix} 78.76 & 72.52 \\ 72.85 & 78.15 \end{bmatrix} * \begin{bmatrix} 0.25 \\ 0.75 \end{bmatrix} = \begin{bmatrix} 74.08 \\ 76.825 \end{bmatrix}$$

To obtain the actual top and bottom die temperatures, reference or ambient temperature should be added with the above. This resistance formulation is valid only for total power of 1W. This LSP formulation was checked with other power levels also. D2-FBGA with board #1 was chosen among the five boards in a sample to get the results for the power level of (0.25,0.75), (0.75,0.25) and (0.5,0.5) to compare the predicted results of LSP. The comparions are shown in Table 6.

Table 6: Mesurement Vs Prediction by LSP

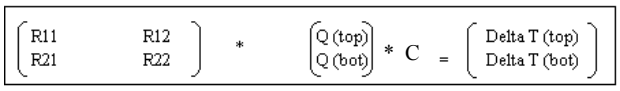
Wind Speed, m/s	Measurement (Board 1) 0.5W @ Both die		Prediction by LSP 0.5W @ Both die		% Error 0.5W @ Both die	
	Delta T (top)	Delta T (bot)	Delta T (top)	Delta T (bot)	Delta T (top)	Delta T (bot)
0	75.89	75.80	75.64	75.50	0.33	0.40
1	63.52	63.39	63.30	63.10	0.35	0.46
2	59.18	58.95	59.33	58.98	-0.25	-0.05

Wind Speed, m/s	Measurement (Board 1) 0.75W Top 0.25W Bottom		Prediction by LSP 0.75W Top 0.25W Bottom		% Error 0.75W Top 0.25W Bottom	
	Delta T (top)	Delta T (bot)	Delta T (top)	Delta T (bot)	Delta T (top)	Delta T (bot)
0	75.40	72.59	77.20	74.18	-2.39	-2.19
1	64.18	61.28	64.82	61.77	-1.00	-0.79
2	59.99	57.12	60.86	57.71	-1.46	-1.02

Wind Speed, m/s	Measurement (Board 1) 0.25W Top 0.75W Bottom		Prediction by LSP 0.25W Top 0.75W Bottom		% Error 0.25W Top 0.75W Bottom	
	Delta T (top)	Delta T (bot)	Delta T (top)	Delta T (bot)	Delta T (top)	Delta T (bot)
0	72.33	74.92	74.08	76.83	-2.42	-2.54
1	61.20	63.57	61.78	64.44	-0.95	-1.36
2	56.70	59.40	57.79	60.26	-1.91	-1.44

Thermal resistance formulation was done based on the mean value of sample size 5. Error was found to be less than 3%. The formulation was also done with all individual board results and the error was still less than 5%. As shown in the Table 6, LSP holds good agreement with experimental resistance matrix formulation. Main limitation of LSP are non-linearity due to radiation and natural buyancy effect in natural convection [1].

In order to account for the non-linearity due to radiation and natural buyancy effect, the formulation needs to be refined with a multiplier 'C' as follows [1]. To get non-linearity component C, thermal performance needs to be obtained for various total power levels.



6. Conclusions

Three-dimensional CFD simulations were adopted to evaluate the thermal performance of D2-FBGA with identical die stack structure. Experimental results of D2-FBGA with 1S0P and 1S2P were validated with the simulation results under still and forced air conditions with 1m/s and 2m/s. The experimental results of ring cold plate test for θjb was also validated with simulation results. All the results were validated within the agreeable limit of accuracy. As two heat sources were involved in D2-FBGA, single thermal resistance value is not applicable. Hence, thermal resistance matrix was generated in a general reporting format for all test conditions to calculate the temperature rise above the ambient and to understand the thermal cross talk between the dies. LSP method was successfully applied to D2-FBGA's thermal performance evaluation and the results were compared with experiments. It was found that LSP method can be used to evaluate the thermal performance of two identical die stacked packages with with reasonable accuracy.

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