Design and Development of True-CSP

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Abstract

"Wafer Level Packaging" has been there in microelectronics industry since late 1990's, but recently it is accepted as package of choice particularly for applications where the pin count is from low to medium. Wafer Level Chip Scale Package (WLCSP) is growing rapidly in consumer application such as cell phone, digital camera and wireless application. It combines the chip scale advantage of small size with efficient production approach based on batch packaging at wafer level. One existing technologies in WLCSP's employ epoxy encapsulation over the pillar bumped wafer and surface polished prior to solder printing. A clear disadvantage of epoxy encapsulation on the whole wafer is the high resultant warpage. With a larger wafer, there is a corresponding requirement to increase the thickness of the wafer during the polishing process in order to relieve high warpage, which could hinder the polishing process. Excessive residual stress induced through the process could result in extensive wafer cracking. This becomes a potential draw back in wafer-level batch processing.

This paper will disscuss an alternate novice method of processing WLCSP by leveraging on existing assembly house equipments. Advantages of this packages, developed by United Test and Assembly Center (UTAC) , would also be discussed. In it's key process, the copper pillar bumped wafer is singulated and attached to a base carrier similar to coventional lead-frame strip. The base carrier strip is then over molded together with the copper pillar wafer before being solder mounted and singulated to its final size. The final package contains base carrier with the chips encapsulated by the compound. Package without base carrier is still under development as an option for ultra thin packaging soulution. This novice package had passed JEDEC Level 3 @ 260 with full environmental test.

This paper also discussed the simulation study using Finite Element Analysis to assess the board-level reliability performance, which is a key concern for CSP structures. Parametric analysis has been included in the study to evaluate the reliability sensitivity of this new package, allowing a better understanding of the mechanical response thus achieving design optimization.

1. Introduction

The race to smaller footprints with increased functionality for the IC is an ongoing challenge. Achieving a good balance between costing and other functional requirements such as the I/O's, quality and reliability, determines the eventual success of the package. Presently in WLCSP world, there are two clear opinions emerging from two groups, Fabs and Assembly houses. One group says that WLCSP packaging should be done at Wafer foundries as most of the activity is done on the whole wafer. The other group says that wafer level packaging can still be done at assembly houses with the minimum infrastructure development. Both arguments have it's pro's and cons. UTAC, being the Test and Assembly house, falls in the latter group.

Figure 1 shows the typical WLCSP process flow and the polymeric encapsulated WLCSP is as shown on figure 2.

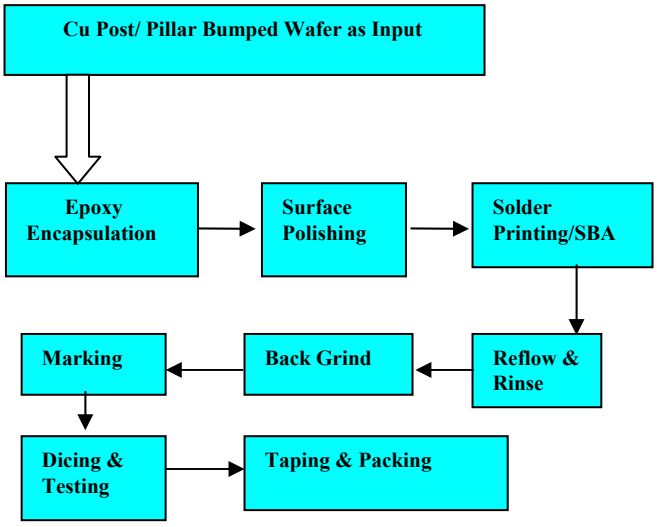

Figure 1: Typical process flow of WLCSP

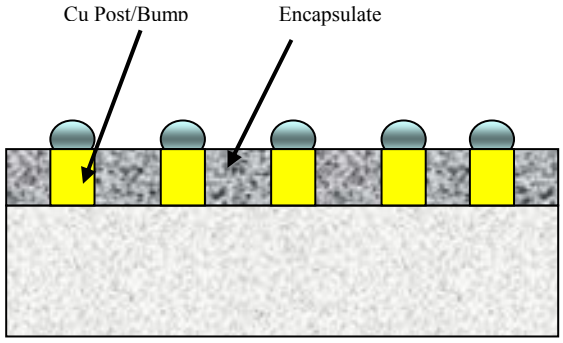

Figure 2 : Schematic view of typical WLCSP

Disadvantages of Wafer Level epoxy encapsulated packages are:

1. After wafer encapsulation, the wafer may have stresses induced due to variation of CTE of silicon and encapsulant. These variations in CTE could result in warpage of wafer or in some case, wafer cracking.

2. Polishing and wafer backgrinding operations could induce further stresses and result in wafer crack, thus has limitation on the backgrinding thickness.

3. Solder ball can be prone to demage during the detaping process.

4. Singulated WLCSP package with bare silicon edge, is susceptible to mechanical shocks in the real world.

UTAC had developed a novice solution using current assembly house infrastructure without incurring any extra investments for wafer level processing. This developed package, called True-CSP, is similar in structure and foot print to normal wafer level package but more robust from it's base carrier feature. It is much easier to handle this package during unit or possible strip level testing. This encapsulated structure is a good alternative to WLCSP, with an added advantage of improved structural integrity.

2. New Package Construction and Assembly Flow

Figure 3 and 4 shows the structure of the two variants of with and without base carrier. The chip size ratio is still maintained within 1.2.

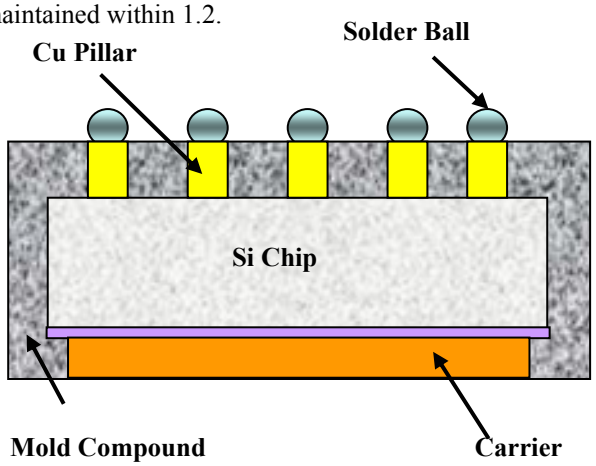

Figure 3 : True-CSP with Carrier (Patent Pending)

In the first variant, the chip is attached to the base carrier using die attach epoxy. Total package height includes the base carrier thickness. The other varient, which is catered for ultra thin package solution, is processed without the carrier. This other novice package is still under development in UTAC.

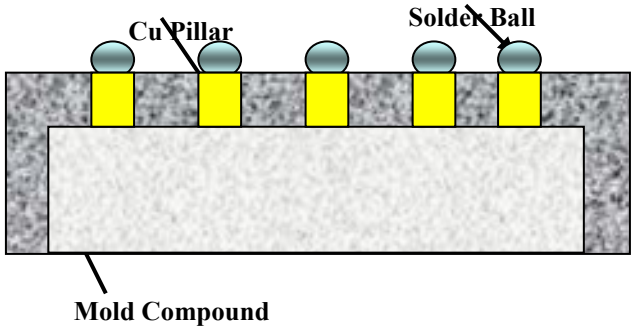

Figure 4 : True-CSP with Carrier (Patent Pending)

2.1 Pillar Bumping Operation

Most of the chips are designed with pad openings for wire bond application. In most of the WLCSP's, the wafers undergo an RDL(Re-distribution layer) process to convert the pheripheral bond pads to an area array pads. This RDL process also helps in the elimination of an interposer (substrate) and it will be able to convert different chip designs to a standard grid array format suitable for customer boards. After the RDL process the wafers are passivated using compatiable polymer coating, for planerization and protection of the circuits. Bumps are grown on the wafer after the UBM sputtering. The UBM acts as an interface between the bump and circular pad openings on the wafer while the pillar bumped wafer acts as an input to the assembly process. 2 types of pillar design (i.e. protruded and embedded) are available and it's design impact on board level reliability is disscussed in detail on Section 3.2.

2.2 True-CSP Process Flow

The process flow for True-CSP is as explained below:

i) Incomming wafers with Cu pillars are back grinded to the required thickness and singulted into individual chips.

ii) The singulted chips are attached onto a specially designed base carrier silimiar to leadframe strip using normal epoxy attach.

iii) This base carrier strip with attached chips is molded using standard mold compound.

iv) Deflashing is done to remove any flash or resin on the exposed bump pads.

v) Solder balls are mounted on the Cu bumps and reflowed.

2.3 Advantages of True-CSP

True-CSP has the following advantages in its unique process flow as compared to typical WLCSP:

1) Ease of processing/handling

While WLCSP is epoxy encapsulated and polished, there is a limit on the bump wafer thickness to be backgrinded. The bumped wafer is subjected to high stress during polishing process and the added wafer backgrinded process can resulted in potential crack or broken wafer. In True- CSP process flow, the stress induced is reduced as the bumped wafer are backgrind and singulated to be attached to the base carrier similar to conventional package.

2) Possibility of Strip testing

True-CSP is processed with the based strip carrier as the base and hence, can have the option to be strip tested from the matrix array of soldered package prior to singulation. This option increases the assembly throughput.

3) Process only known good die and cost effective

In WLCSP, the whole bumped wafer is epoxy encapsulated including the rejected units. This resulted in waste material and processing time to separate out the good units in the downstream process. In the True-CSP process, only known good die will be attached to the carrier (by wafer mapping) to eliminate the tedious segregation process in the down stream process. This is cost effective and it improved production efficiency.

4) No major investment needed

True-CSP can make use of standard assembly equipment for the assembly process and hence, does not require major investment to manufacture the Chip Scale Package.

5) Robust mechanical structure

The True-CSP package construction consists of copper pillar die attached above the base carrier and protected by compound on all side of the die for mechanical robustness. This structure enabled better drop test strength and is well protected during electrical testing or board level mounting

3. Package Performance Assessments

3.1 Package Level Reliability Tests Results

Reliability tests on True-CSP were conducted at the package level to assess its internal structural integrity and interfacial delamination by acoustic scanning electron microscope (SAM). All units passed Jedec Level 3 @260C with all the environmental testing. Figure 5 below shows the summary of reliability and environmental result.

		Results	
Test	Condition (JEDEC Std)	F/SS	No of Cyc / hrs
MSL	30°C/60%RH, 192 hrs	0/66	Passed
TC	-65°C to +150° 2 cycles/hr (JESD22-A104-B)	0/22	Passed 1000 cyc
PCT	121°C / 100% RH 2 atm (JESD22-A102-C)	0/22	Passed 168 hrs
HTS	150 °C (JESD22-A103-B)	0/22	Passed 1000 hrs

Figure 5: Summarised reliability test for True-CSP

Figure 6 and 7 below show the through scan and cross section of the True-CSP after the Level 3 preconditioning testing respectively and no delamination was observed on the interfaces.

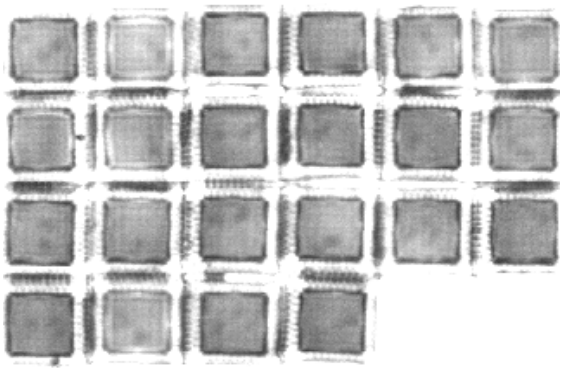

Figure 6: Through scan after L3 preconditioning

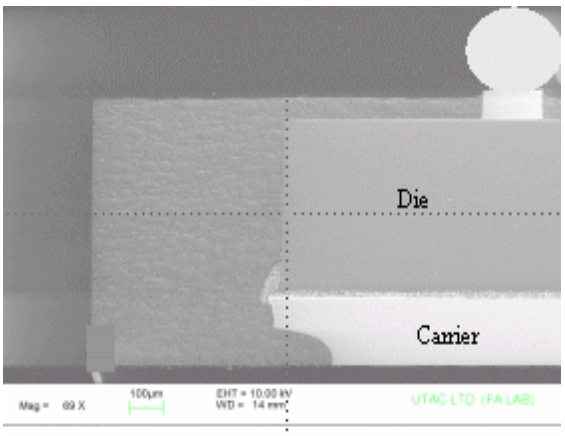

Figure 7 Cross section of reliability units after L3

3.2 Board-Level Solder Joint Reliability

True-CSP and other chip-scale packages provide the benefit of small footprints under the usage of standard die size requirement. Board reliability information is essential for True-CSP implementation especially for high reliability applications. Under the high I/Os yet finer pitch requirements, the board-level solder interconnect is expected to come under higher stress giving rise to greater concern on the system's functional integrity. Prior to development of True-CSP, study based on Finite Element Analysis (FEA) was performed to study the impact of design variations on board-level reliability. While physical accelerated temperature cycling (T/C) test remains an essential component to evaluate the board-level reliability of trueCSP; FEA provides a fast and effective platform for design optimization, eliminating extensive Design of experiments during the course of package development.

Common findings in the literature have shown similar failure mechanism in wafer-level CSP typical of Ball Grid Area (BGA) packages. Solder-joint damage in the form of fatigue cracking has been widely reported to remain the prime cause of failure under temperature cycling. Solder cracking is associated with the thermal expansion mismatch of the package and PCB materials, resulting in fatigue straining within the solder interconnect. In the current study, solder fatigue under temperature cycling condition forms the main scope of board-level reliability analysis. In order to establish a common basis of comparison, standard 62Sn/36Pb/2Ag eutectic solder material has been used for the current study. Based on package symmetry, a parametric 3D half-diagonal strip model has been constructed, which covers adequate representation of the critical joints along the distance from neutral point (DNP). The detailed Under Bump Metallizations (UBM) has not been included in the model. The model is subjected to a temperature cycling condition of -40°C to 125°C, with 15 minutes ramp and dwell at 1 cycle per hour. Darveaux's [3] viscoplastic methodology has been adopted for the current solder fatigue analysis. Shown in figure 8 below is the strip model for True-CSP with the base carrier. This option will be used a benchmark across all parametric studies.

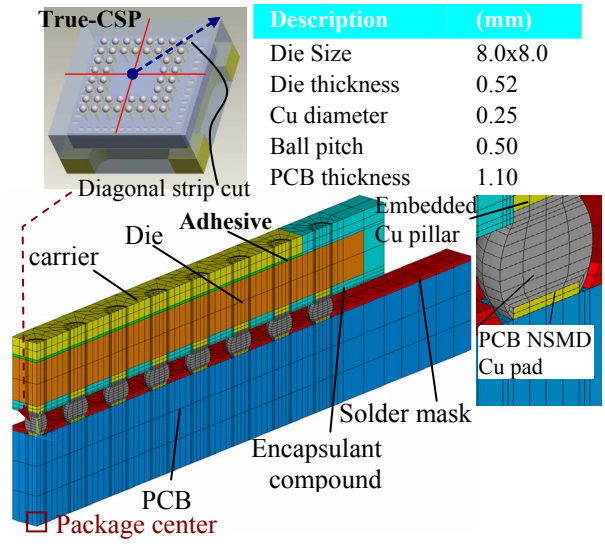

Figure 8: FEA diagonal strip model

Shown in figure 9 below is the contour distribution of energy density (plastic work/volume) for the solder joints that are near to the edge of the die. The solder ball that is nearest to the die corner has been observed to sustain a greater degree of plastic work and the intensity is especially pronounced at the package side solder interface. It is envisaged that the solder ball near to the die corner is at a higher risk of fatigue failure under T/C condition.

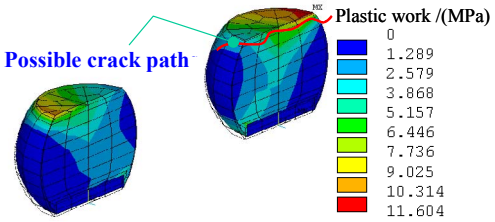

Figure 9: Energy density of solder joints near die

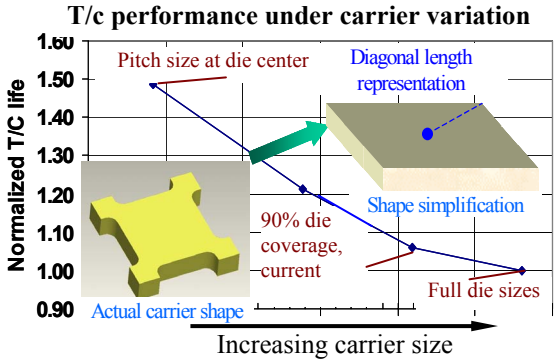

Figure 10: Effect of carrier size variation on solder fatigue life

3.2.1 Global Design on Solder Fatigue Reliability

Base carrier serves as a secure during strip-saw. However, with this additional coupling to the die, it would be necessary to investigate the impact of base carrier on solder fatigue performance. Using Cu material for common lead-frame application, it is observed that the carrier size has a significant impact on the solder fatigue performance, especially for the

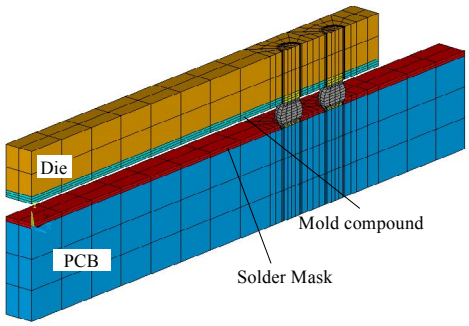

Figure 11. Diagonal strip model for True-CSP w/o carrier

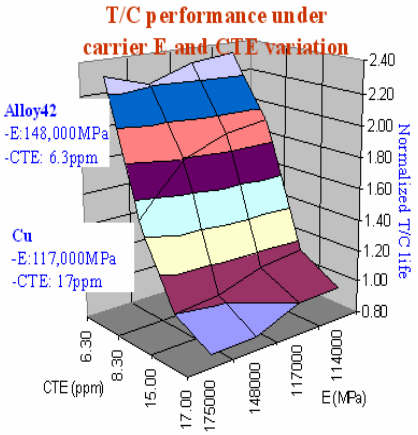

Figure 12: Sensitivity of solder fatigue life under carrier material variation

critical ball. As shown in figure 10, the normalized fatigue life increases as the carrier size decreases. Silicon die has the lowest coefficient of thermal expansion (CTE) amongst all packaging components and this governing CTE mismatch creates significant straining in the solder joints (in predominately shear mode along the adjoin solder interface). By introducing a carrier at the die back, the entire package comes under greater CTE mismatch during temperature loading. It is thus of great interest to explore other channels of improvements based on the True-CSP option with base carrier.

A sensitivity sweep for the choice of carrier material was performed. It can be observed in figure 12 that the CTE of carrier material has a more significant impact on the fatigue life of solder joints under temperature cycling. As an offhand reference, material such as Alloy 42 is expected to be a better option compared to common Cu material in terms of solder fatigue performance. It is thus necessary to select a material with better matching CTE with the die in order to reduce mismatches under T/C loading. The True-CSP option without the carrier under development as shown simulated in figure 11, is an alternative measurement to enhance solder fatigue performance. Based on simulation prediction, without the presence of a carrier, the fatigue life of solder joint is expected to increase by 2.5 times. Other design parameter includes the die thickness. As shown in figure 13, the solder joint fatigue life decreases as the die thickness increases within the range of current study. On the other hand, the impact coming from a thicker die saturates within close rang

of two times current die thickness. Other design parameters could be the resultant bottleneck beyond this range.

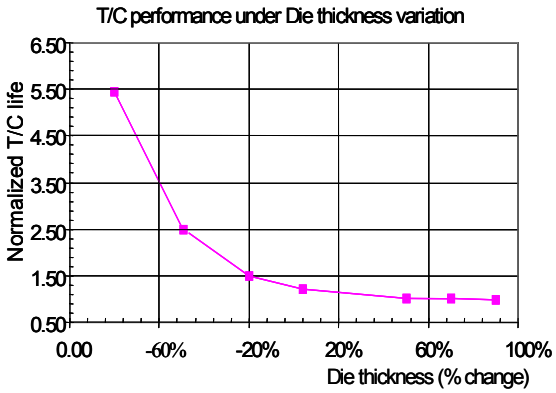

Figure 13: Effect of die thickness on solder fatigue life

3.2.2 Local Design Consideration

Other design consideration pertains to structural layout near to the solder interface, which have direct impact on solder fatigue reliability. The Cu pillar-solder interface design is subjected to taping and molding process control. Referring to figure 14, two main variants would be of interest, namely the embedded pillar design (which resembles Surface Mask Defined pad design in conventional package) and protruded pillar design (which resembles Non-Surface Mask Defined pad design). Based on analysis, True-CSP with protruded pillar design is observed to yield a fatigue life of approximately 1.44 times compared to the embedded pillar, which has been adopted in the analysis benchmark. It is postulated that the protruded pillar design reduces shearing along the pillar-solder interface through a re-distribution of stress (and thus lower damage represented in the form of energy density). The embedded pillar design may be a more promising option in enhancing solder fatigue performance. Other design consideration includes the sensitivity of Cu pillar height. Referring to figure 15, solder reliability is observed to decrease by about 15% when the pillar height decreases by half. This trend is expected of common intuition since the solder interface becomes nearer to the die and will be subjected to greater shearing under the influence of global CTE mismatch.

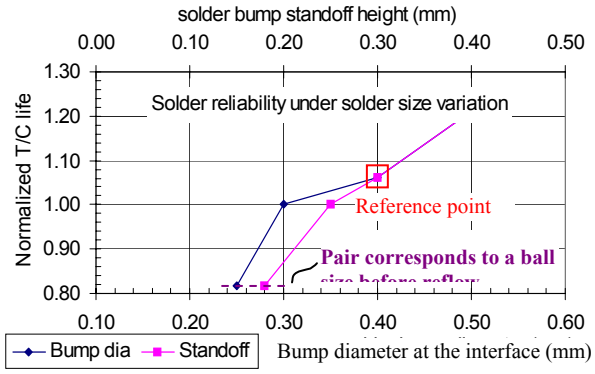

Figure 16: Effect of solder size on fatigue life

The solder profile provides another channel to evaluate solder fatigue reliability. Shown in figure 16 is the combined effect of pillar diameter (which governs the diameter of solder at the pillar-solder interface) and solder standoff height on solder fatigue reliability. A decrease in pillar diameter and height will correspond to a decrease in solder fatigue life. While the pillar diameter affects the stress intensity distribution of solder bulk near to the pillar-solder interface, pillar height determines the proximity of solder interface to the die, which governs the extent of shearing at the interface under the influence of global CTE mismatch. Depending on the severity of global CTE mismatch, an increase in pillar diameter may provide a better enhancement of solder fatigue reliability compared to solder bump height based on per dimensional variation.

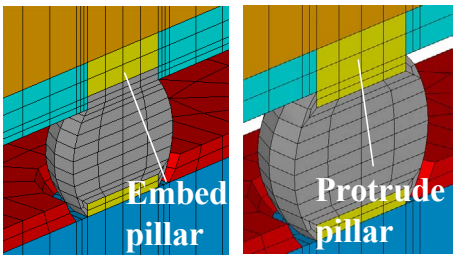

Figure 14. Illustration of embedded and protruded pillar design

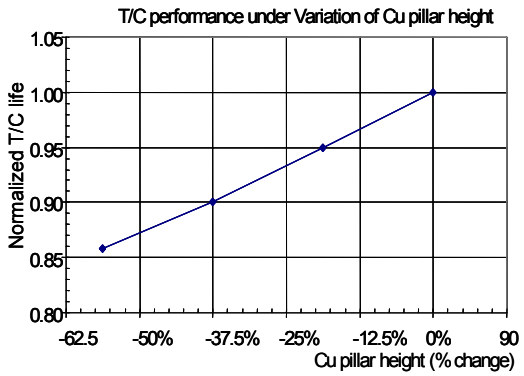

Figure 15 Effect of pillar height on solder fatigue life

4. Heat Dissipation and Thermal Performance

In new package development, it is essential to assess the heat dissipation capability of the package. Thermal modeling was carried out using Flotherm 4.1 to determine its thermal resistance, θ_{JA} (^{o}C/W), with values shown in Figure 17. A device power of 1.5W with ambient temperature of 50^{o}C was used. The still and forced air convection conditions followed Jedec standards of JESD 51-2 and JESD 51-6 respectively, with the package mounted onto a 4L PCB (JESD 51-9 defined). Packages of 5x5mm (I/O count of 64) and 8x8mm (I/O count of 225) were simulated to account for the difference in package size on thermal performance.

	Air Flow (m/s)	Theta Ja (°C/W)	
		5x5mm	8x8mm
True-CSP-1 (with carrier)	0	37.1	18.1
	1	32.6	14.3
	2	31.1	13.5
	3	29.6	12.8
True-CSP-2 (w/o carrier)	0	37.9	18.3
	1	33.6	14.5
	2	32.1	13.6
	3	30.8	12.9

Figure 17. Thermal simulations data of θ_{JA} (°C/W) for True-CSP package.

Thermal simulation comparison between two different concepts of True-CSP – with and without carrier for 5x5mm and 8x8mm package sizes has revealed comparable thermal performance. With a larger package size, effective heat dissipation away from the package will be enhanced with increased number of solder balls and a larger die surface. A θ_{JA} of 18 °C/W is achievable for the 8x8mm True-CSP.

5. Conclusion

UTAC has successfully developed an alternate approach to WLCSP process by leveraging on existing assembly equipment infrastructure to produce Patent Pending True-CSP. In comparison with typical Wafer Level Package, it has advantages such as ease on handling, lower material cost, robust mechanical structure and required no major investment.

Thermal simulation shows that there is no difference in thermal performances between base and baseless carrier True-CSP. However, the design of Cu pillar and package configuration is critical in enhancing the board level reliability based on Finite Element Simulation. Parametric analysis shows that the Cu pillars structure, diameter and die thickness play significant impact on enhancing the solder joint reliability.

6. Future Work

The second design of True-CSP without base carrier is still under development. These units will also be subjected to higher level of reliability testing and result will be reported upon completion.

Experimental board level solder joint fatigue life will be correlated with simulation results.

Acknowledgments

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