# Stacked Die Technology Solutions for wCSP Memory Packages

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## Abstract

*Due to an expanding consumer electronics market and the need for form factor reduction, stack packages have been gaining popularity in the last 3 years. The most efficient way to increase memory product's capacity without increasing package size is to adopt die stacking package structure. Essentially, DRAM's layout is different compared to other chip option – the bond pads are located on the chip centerline. Conventional die stacking structure might not be suitable for DRAM packaging application. This paper presents three innovative package designs for DRAM memory packages, with the option of die stacking: D2i/D2-wCSP, D2-FBGA and 2DD2-wCSP. This paper discusses the scope of development for these packages, comprising of upfront design considerations such as electrical performance, package structure design and reliability. Assembly process and development will also be discussed. Finally package reliability and board level reliability data are also provided in this paper.*

Key words: Window Chip Scale Package, Stack die, DRAM, Board-level reliability, package development

## Introduction

Window Chip Scale Package (wCSP) is a special package structure for DRAM application, in which the bond pads are all locating on chip centerline (Refer to Figure 1)[1]. Under the requirement of die stacking, the resultant die-stacked structure is different compared to traditional die-stacked packages. For a 2-die stacked wCSP structure, the active face of the top die faces upward while the active face of the bottom die faces downwards as shown in Figure 2. Under UTAC's naming convention, this package configuration is termed as D2i-wCSP, in which the 'i' represents the interposers. The interposers facilitate to bridge the interconnection between the center of the die to the substrate avoiding the requirement for long wire bonding.

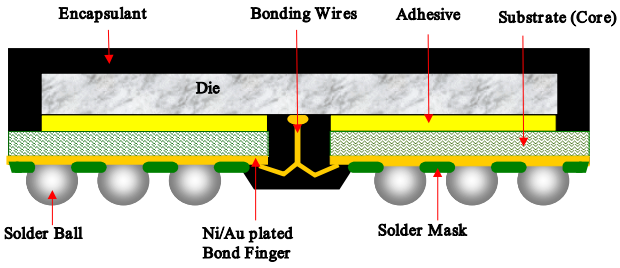



**Figure 1: Typical wCSP package structure**

Where die size, bond pads layout or package size are allowable, it is possible to remove the interposers from the top die, relying on wire bonding to furnish the interconnection between the top die and substrate directly. Show in Figure 3 is an illustration of the D2-wCSP package structure.

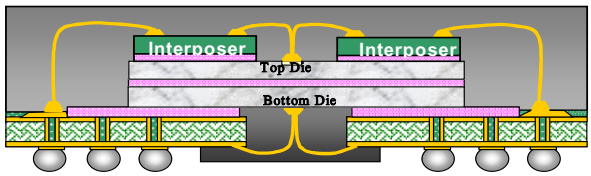



**Figure 2: D2i-wCSP package structure with interposers.**

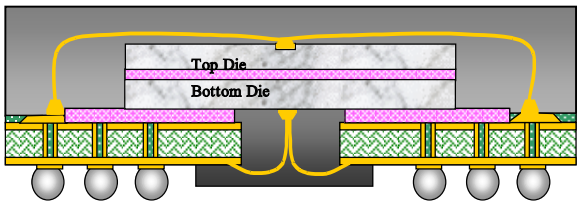



**Figure 3: D2-wCSP package structure without interposers.**

D2(i)-wCSP presents a suitable packaging option for memory device with a single row of bond pads. With the increase of memory density and thus greater I/O connections requirement, package design would need to accommodate possible memory chip design with two rows of bond pads. D2(i)-wCSP stacked die structure will be less of an ideal structure for chip design with two rows of bond pads. Under the consideration of Mirror effect, the pads on the bottom die have to be routed from one side to the other side of the substrate in order to establish connection to their respective matched pads on the

top die. The implication of cross routing will make substrate design extremely difficult and almost impossible under high I/O connection. Therefore, for high I/O memory device with two rows of bond pads, there is a need for innovative stacked structure, which allows the top and bottom dies to align in common direction within the package.

Shown in Figure 4 is the package structure for D2-FBGA, which possesses the above mentioned advantage compared to D2(i)-wCSP. This package design allows the active faces of the two stacked dice to align upwards. Because two dice are facing the same direction inside the package, also there is not any window slot needed on the substrate, the substrate routing problem can be solved.

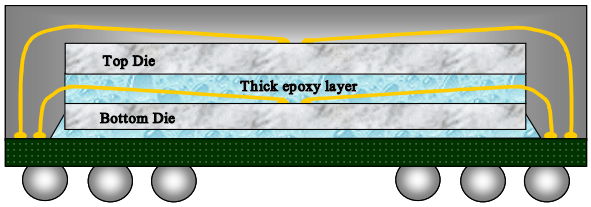



**Figure 4: D2-FBGA package structure with both dice facing package top direction.**

Although D2-FBGA can solve the drawback of D2i/D2-wCSP on substrate design, good electrical performance is critical for package solution selection. In general, low parasitics of resistance (R), inductance (L) and capacitance (C) are desired. However due to the inclusion of additional die for increased memory capacity in a single package, simultaneous achievement of both net length matching between the top/bottom dice and low capacitance has to be compromised. For instance in D2-FBGA design, low capacitance is achievable in the expense of high inductance in some signal pins (although with matching net length). As for the D2i-wCSP version, lower inductance can be achieved for the bottom die but with non-matching net length with the top die and a higher capacitance. Another version of 2DD2-wCSP package is developed, as shown in Figure 5. This package contains two stacked dice with the active faces in line with the package bottom. Compared with D2-FBGA, all the long bonding wires are replaced by metal traces inside the substrate thus resulting in a lower inductance. It also provides a better net length matching between top/bottom dice with a lower capacitance when compared to the D2i-wCSP package. More considerations in package selection for electrical performance will be discussed in the subsequent section.

## Assembly Process

D2i/D2-wCSP

The manufacturing process of the D2i-wCSP package is similar to the D2-wCSP except the inclusion of the interposers attachment which acts as the bridge of long wire interconnection. The assembly process flow is shown on Figure 6.

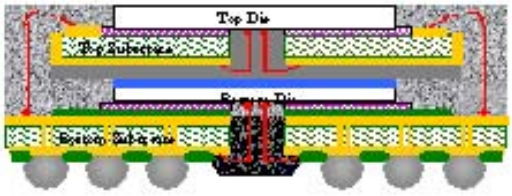



**Figure 5: 2DD2-wCSP package structure with both dice facing package bottom direction**

Due to the presence of interposers, D2i-wCSP will have a higher material and process cost compared to D2-wCSP. Also, under the same package height requirement, D2-wCSP can accommodate a thicker die thickness, presenting a lower process risk and costing due to wafer backgrinding and wafer mount process steps. However, D2-wCSP needs tight wire looping control for wire bonding on the top die as the long wires need to traverse a larger part of the die surface to die center. Long wire poses a challenge to the molding process in terms of wire sweeping control. Figure 7 shows the SEM images for D2(i)-wCSP prior to the molding process.

D2-FBGA

The manufacturing process flow of D2-FBGA is almost the same as the one for conventional stacked die package. However, there are several main challenges faced in the D2-FBGA process and they are briefly described below:

1. Material selection for DA epoxy between top and bottom die

As the long bonded wires need to go through two types of epoxy materials – DA epoxy and mold compound, therefore, it becomes critical to evaluate the top die attach epoxy with the requirements as follow:

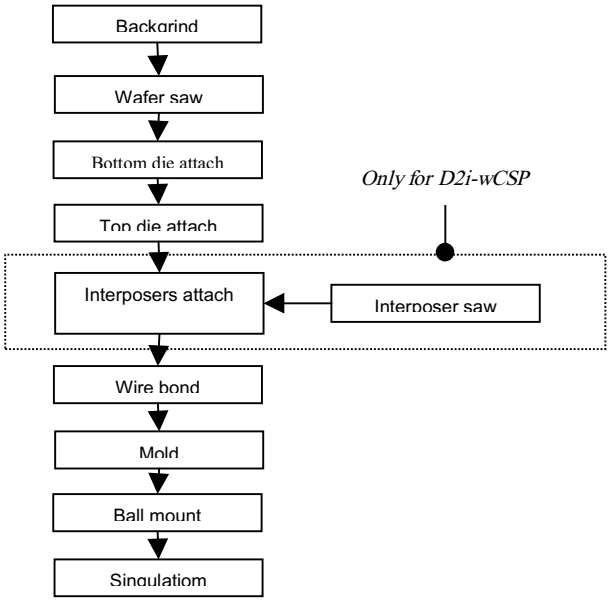



**Figure 6: Assembly process flow for D2i/D2-wCSP.**

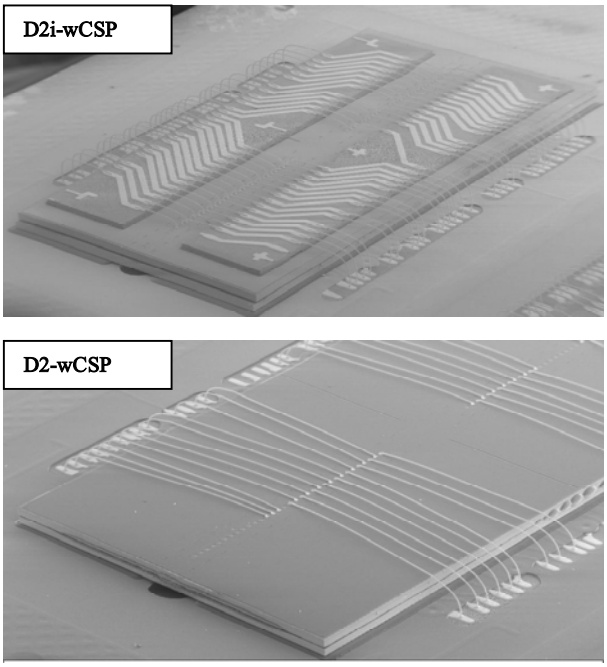



**Figure 7: SEM photos for D2i/D2-wCSP.**

- Low shrinkage after cure. As high shrikage of epoxy will cause additional stress to bonded wires, and lifted or broken wire may happen.
- Try to reduce the mismatch of CTE with mold compound. Delamination may happen due to mismatch of CTE between DA epoxy and mold compound, and this delamination may tear the wire to be broken during TC test.

Figure 8 illustrates some scenarios of DA epoxy with various degrees of shrinkage and the separation resulted by material shrinkage and CTE mismatch with other package material.

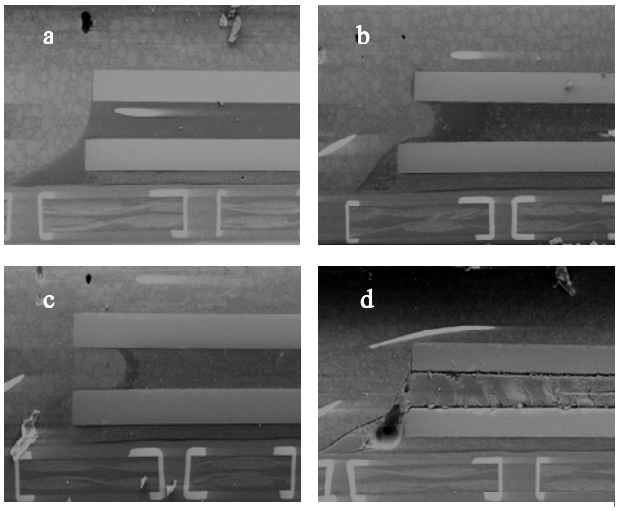



**Figure 8: DA epoxy's shrinkage after cure and CTE mismatch with mold compound.**

a) Epoxy a has not any shrinkage after cure.
b) Epoxy b has a slight shrinkage after cure.
c) Epoxy c has serious shrinkage after cure.
d) Epoxy d has high CTE mismatch with mold compound, and separation was happened on the interface.

2. BLT (Bond Line Thickness) control for DA epoxy between top and bottom die

Compared with BLT of conventional die attach process, which is around 1mil (25um), in this D2-FBGA much thicker epoxy layer is required for die attach between top and bottom dies, in order to accommodate enough space for wire bonding loop on the bottom die. Based on process evaluation in UTAC, 160um Bond Line Thickness is needed for 4.5 to 5mm long wires on bottom die.

3. Wire-sweep control for bonded wires on top die during molding process

In order to reduce wire sweep for bonded wires on top die, several factors need to be considered: design to allow mold flow in alignment with the mold gate and wire span in the same direction as well as optimization of molding parameters. Within the limit of package height allowance, additional interposers can be incorporated on the top die surface which help to promote shorter wire length as in D2i-wCSP.

2DD2-wCSP

2DD2-wCSP is the most complicated stacked die package, using package in package concept. Figure 9 is its assembly process flow:

1. Top die is attached on top substrate and wire bonded.
2. Top die portion is molded and singulated to be a package.
3. Bottom die is attached on bottom substrate and wire bonded.
4. Top package is attached on bottom die, and following the same direction as bottom die – facing package bottom surface.
5. Finally mold the whole package.

SEM photos of package structure are shown in Figure 10.

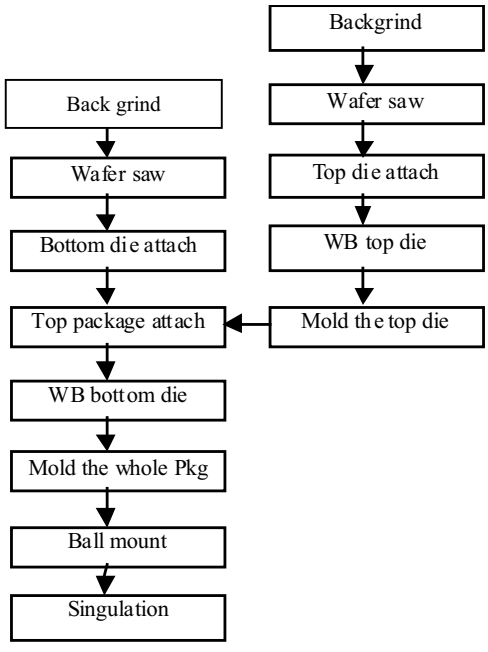



**Figure 9: Assembly process flow for 2DD2-wCSP**

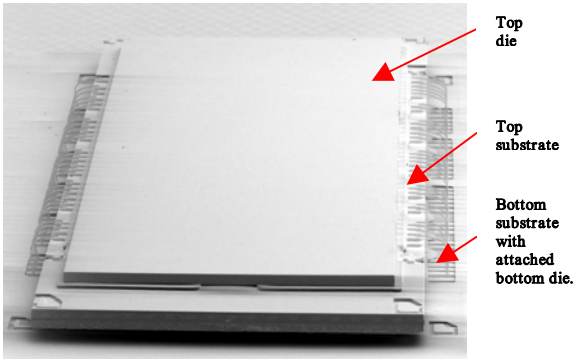



Figure10: SEM photo for 2DD2-wCSP

## Electrical Performance Considerations

Good electrical performance is a key driving factor for selecting a suitable package design. Low electrical parasitics in resistance (R), inductance (L) and capacitance (C) of an IC package are desired. In the current proposed stacked die memory packages, it is important to understand the electrical characteristics of each package type in meeting different customers' requirements and applications. A 3-dimensional (3D) electrical simulation was performed using Ansoft Spicelink, with the package parasitics of RLC compared in Table 1. The packages modeled were D2i-wCSP, D2-FBGA and 2DD2-wCSP, with a common package size of 11.4x12.5mm and a die size of 9.32x9.49mm (dual center bonding pads). Three nets of "CLK", "DQ2" and "DQ15" were selected for analysis, with each net consisted of connection from the top/bottom dice and routed according to the respective package design. The solder ball pin assignment is assumed to be the same for all three packages. The respective 3D simulation models are shown in Figure 11.

**Table 1: Comparison of RLC for different package types.**

| Pk Type | Net | R (mOhm) | | L (nH) | | C (pF) |
|---|---|---|---|---|---|---|
| | | Top | Bot | Top | Bot | N.A. |
| D2i-wCSP | CLK | 270 | 80 | 7.91 | 2.39 | 0.58 |
| | DQ2 | 260 | 60 | 7.02 | 1.57 | 0.54 |
| | DQ15 | 390 | 120 | 15.6 | 3.84 | 0.61 |
| D2-FBGA | CLK | 440 | 420 | 8.61 | 7.39 | 0.14 |
| | DQ2 | 400 | 390 | 9.11 | 8.81 | 0.15 |
| | DQ15 | 440 | 430 | 12.45 | 12.3 | 0.17 |
| 2dd2-wCSP | CLK | 200 | 76 | 6.21 | 2.28 | 0.28 |
| | DQ2 | 221 | 56 | 6.78 | 1.49 | 0.32 |
| | DQ15 | 183 | 103 | 6.84 | 3.71 | 0.28 |

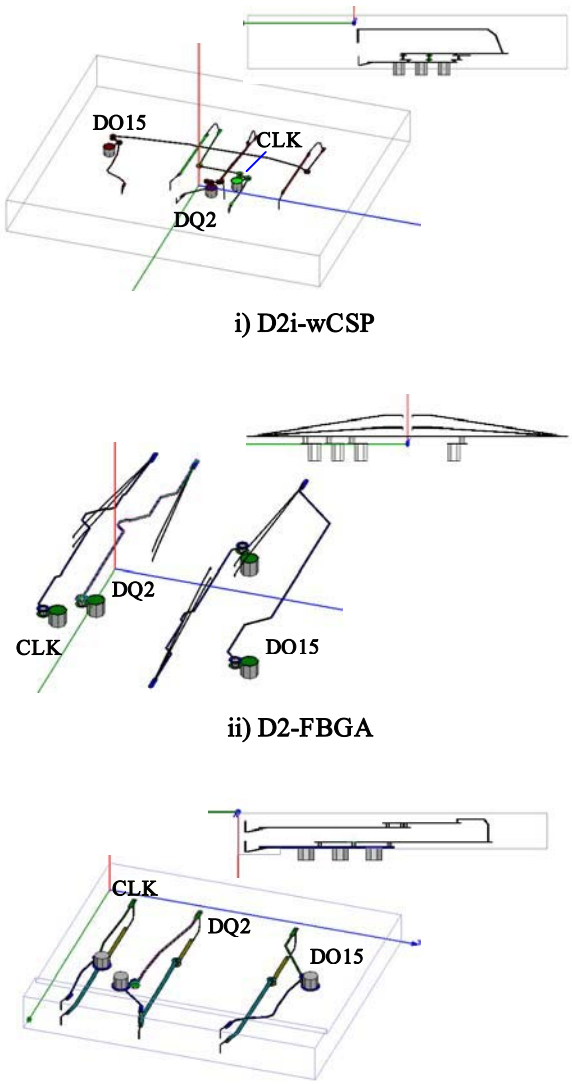



**Figure 11: 3D models for i) D2i-wCSP, ii) D2-FBGA, iii) 2DD2-wCSP.**

In the D2i-wCSP design, a similar die is being flipped over and stacked onto the bottom die. As explained in the preceding section due to the result of mirror effect, the pairing pin of the top die (for instance "DQ15") has to be routed from one side to the other side of the substrate for the connection with its matched pin on the bottom die. Long connecting trace has to be routed on the substrate thus resulting in a high inductance (L = 15.6nH). Although low inductance can be achieved for the bottom die, the resulting mismatch in the inductance of the pairing pin may affect its electrical performance and integrity of the signal.

With the D2-FBGA design where both dice are facing upwards, the direct wire bonding method will provide a much better match in the trace length of the paring pin thus resolving the mismatch issue in inductance. It can also be seen that the capacitance of the three nets is the lowest among the

three package types. The only concern lies with the higher inductance contribution. In the top die where a longer bond wire is needed, the inductance will be higher than a net that is formed by copper trace (per D2i-wCSP design, "CLK" and "DQ2" nets). With the additional need of routing from one to the other side of the substrate due to commodity pin assignment conformation, the extra trace length gave rise to an increase in the inductance (significant increase in the bottom die). Nonetheless in the case where the inductance values meet customer specifications, the matching inductance will provide an optimal electrical performance.

The 2DD2-wCSP can be viewed as an accommodating design where an improvement of the capacitance can be achieved over the D2i-wCSP design, at the same time providing better inductance matching. Using "DQ15" net as an illustration where the two stacked dice are facing down, the routing of the long trace for the top die is being eliminated thus resulting in a lower inductance (L decreases from 15.6nH to 6.84nH). When compared with D2-FBGA, the long bonding wires are replaced by metal traces inside the substrate for the 2DD2-wCSP package. Hence inductance decreases as a result ($L_{wire} > L_{copper\ trace}$). From the above observations, the 2DD2-wCSP design offers a good package solution for concurrent electrical requirements of low inductance, low capacitance, and closely matched net lengths. The above investigation revealed the different electrical characteristics of the three package types. Hence careful selection of a package solution is necessary in meeting customer specific electrical requirements.

## Package Level Reliability

All the above mentioned stacked die packages, including D2(i)-wCSP, D2-FBGA and 2DD2-wCSP went through UTAC package level reliability tests, and they all did pass the tests. Below are the criteria of reliability tests.

*MSL3*: 30°C/60% RH, 192 hours; 3xIR reflow with 260 °C. Sample size = 135 units.

*Temperature Cycling*: -65 °C/150 °C with 1000 cycles, 0.5 hour/cycle. Sample size = 45 units.

*High Temperature Storage*: 150 °C with 1000 hours. Sample size = 45 units.

*Autoclave*: 120 °C/100%/2atm with 168 hours. Sample size = 45 units.

## Board-Level Reliability Consideration

Package assemblies are exposed to a wide range of external loadings both in the phase of production as well as during field usage. For BGA packages, solder joints provide both the electrical and mechanical connections between the device and the printed wiring board (PWB) module. Thus, damage to solder may readily affect a system's functional integrity.[2,3,4] Solder fatigue reliability during temperature cycling (T/C) is an important qualification requirement which determines the suitability of the package for on-board application. To date, actual accelerated T/C testing had been conducted on D2-wCSP while testing for the other package types are under development. Upfront analyses using the Finite Element Method were also performed in consideration of package optimization at the design stage, prior to the implentation of actual T/C test, which can be time consuming, hitting on the time line of product development.

Board-level T/C reliability of D2wCSP

In the current test vehicle, a sample size of 32 units were included in the test matrix to provide adequate determination of the weibull slope and the characteristic life. The package was daisy chained to the die with full joints monitoring on the board side.

Shown in Figure 11 below is the specification of the package build. The solder joints were of 63Sn/36Pb/2Ag composition with a ball diameter of 0.45mm prior to reflow. The packages were surface mounted onto a PWB, which can accommodate 12 units (with individual isolation slots) per panel. The package integrity was assessed prior to the temperature cycling test with a range of –40 °C to 125°C, with ramp and dwell loads at 15 minutes interval each at approximately 1 cycle per hour.

| | |
|---|---|
| **Package Type** | :D2-wCSP 90B; Size: 13.0x8.0x1.2 mm |
| **Die quantity** | :2 similar die |
| **Die Size** | :5.016 x 9.732 x 0.140 mm |
| **Substrate** | :UTAC design daisy chain to die |

**Figure 12: Specification of D2-wCSP**

Based on the current test-setup, D2-wCSP achieved a T/C characteristic life of 1697 cycles as shown in the Weibull plot of Figure 13. All failures had been verified to be solder failure due to ball joint cracking (see Figure 14). Prior to actual testing, a numerical model based on the exact package setup was analyzed. Shown in Figure 15 is a quarter model of the D2-wCSP. Darveaux's methodology [5] was implemented for the current analysis. Numerical prediction showed a T/C life of 1,468 cycles, achieving an accuracy of within 13% compared to the actual T/C result. Similar methodology with the same material set was extended to the analyses for 2DD2-wCSP and D2-FBGA. Figure 16 shows the half-2D view of the respective models. 2DD2-wCSP showed a higher reliability (close to 10% increase) compared to D2-FBGA and D2wCSP, which were observed to yield comparable performance in terms of board level T/C reliability. This trend provides upfront comparison for the 3 different package designs, in aid of better design focus during the development stage. Actual performance remains to be validated.

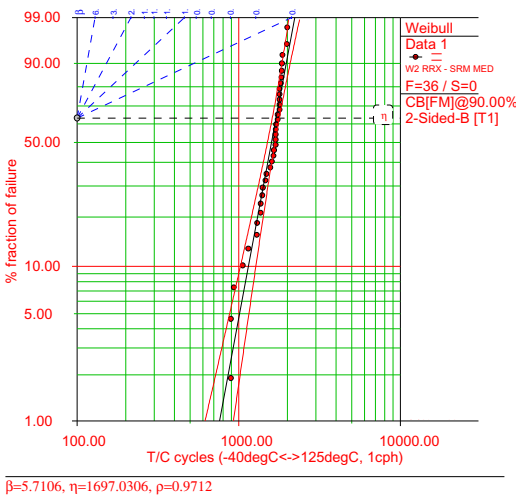



**Figure 13: Weibull distribution for D2-wCSP**

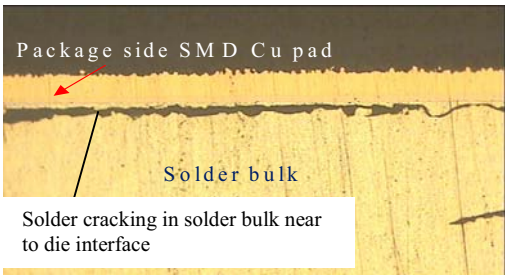
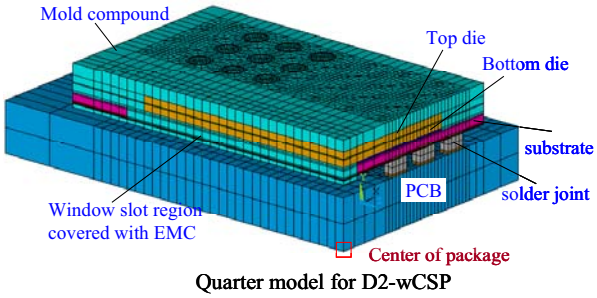
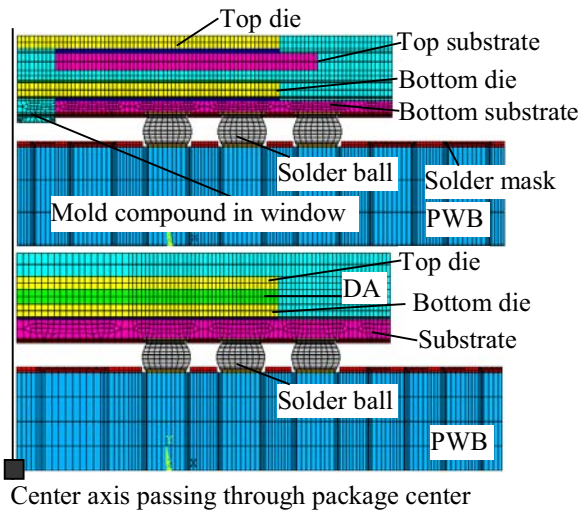



**Figure 14: Optical micrograph showing solder crack.**




Quarter model for D2-wCSP

**Figure 15: Quarter model for D2-wCSP**




Center axis passing through package center

**Figure 16: Half 2D view of 2DD2-wCSP and D2FBGA**

## Conclusions

This paper presents the different options for a stacked die memory package, with the various aspects of assembly process, package reliability, board level solder joint reliability and electrical performance being addressed. The work outlined the challenges in the assembly process, the comparison of solder joint fatigue lives under thermal cycling test, and the packages' electrical characteristics. Recommendation for suitable package solution will be dependent on customers' requirements and applications, along with others considerations such as ease in assembly, materials availability and selection, cost and package performance.

## Acknowledgements

The authors would like to thanks the following Research and Development Group members for their design and engineering contribution to this paper: CK Wang, Joanne Teo, Thomas Chiah, Teng Loy Sing and Tan Hua Hong.

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