Reliability Assessment of a High Performance Flip-Chip BGA Package (organic substrate based) using Finite Element Analysis

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Abstract

The continuous rise in performance requirements of high-end computers and networks has resulted in a rise in demand for high pin count and more sophisticated thermal solutions. Flip chip technology naturally presents a good option in offering I/Os of more than 500. With the addition of a heat spreader (of either one-piece or two-piece lid), the thermal performance of the package can be improved tremendously. However due to the differences in material type for one-piece and two-piece designs, the mismatch in thermal expansion between substrate and lid has constituted to different stress distributions in the package. In the current work, finite element simulation was used to perform structural analysis and comparison between the two different designs. Results showed that the two-piece design generated a lower package warpage, thus allowing better surface mounting. On the other hand, the one-piece lid constituted to lower package induced stresses. The increase in lid width improves package performance in terms of warpage and heat spreader to substrate interfacial shear stresses. Solder joint reliability for the one-piece design was evaluated using Darveaux's volume weighted average viscoplastic strain energy approach. To account for the effect of ramp rate and frequency effects of a temperature cycle, frequency-modified low cycle fatigue relationship developed by Shi et al was employed for comparison with Darveaux's computation. Lastly, parametric effects of lid material, bond pad structure, die size, substrate and PCB thickness on solder joints reliability have been documented. The trends presented would be useful for both the package and board level reliability assessments and containing possible solder joint failures.

1. Introduction

With the drive towards cutting edge technology for Internet communications and high-performance computing applications, the demand for high-end computers and powerful network systems is increasing. Conventional plastic ball grid array packages are not able to meet the high pin counts and large heat dissipation requirements. Existing flip chip technology is capable in meeting I/Os of more than 500. The attachment of a metallic heat spreader (with thermal interface material of high thermal conductivity) over the flip chip enables large amount of heat to be dissipated away from the package top. Two choices of heat spreader design are currently available in the market – the two-piece and one-piece lids. As shown in Fig. 1, the two-piece lid comprises of a stiffener and a top lid. Whereas in the latter design, the stiffener ring is integrated with the top lid utilizing the fabrication technique of powder injection molding. The two-piece type allows better design flexibility as the stiffener can be made with different widths, allowing dimensional change in die size. Recently the one-piece design has gained its popularity, due to a reduction in piece part and adhesive cost, processing steps and handling time. However there exist several concerns in the stress distribution between the one-piece and two-piece designs. Firstly the two designs are structurally different, and require different material processing steps. The one-piece lid is normally fabricated using powder injection molding with base material of either aluminum silicon carbide (AlSiC) or copper graphite (CuC), while the two-piece lid can be made by etching process of copper based material with nickel matte finish. The latter also requires different bonding adhesives with a longer lid width (as compared to one-piece design of a similar package size). Secondly, *coefficient of thermal expansion* (CTE) mismatch between the lid and substrate will give rise to different induced stresses in the package. With a CTE of 17 ppm/^{o}C, copper based lid will be more compatible with organic BT substrate (& CTE of AlSiC equals ~ 9 to 11 ppm/^{o}C). Package warpage will also cause difficulty in board surface mounting. Lastly, board level solder joints' reliability will be impacted by the selection of different lid types and materials.

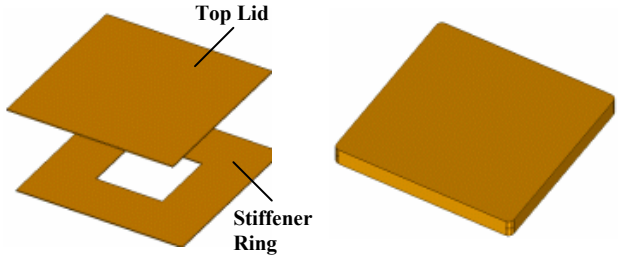


Fig 1. Designs of Two-Piece and One-Piece Lids.

Solder joints fatigue performance has always presented a concern in IC packages development. With the inexpensive means of numerical method, finite element analysis (FEA) is being used for solder joints reliability assessment in many thermally enhanced flip chip BGA packages [1-3]. Generally the strain energy density representing the damage per cycle of the solder joint can be extracted. The well-established volume average viscoplastic strain energy fatigue life model developed by Darveaux [4,5] has been widely employed in the electronic packaging industries for board level reliability assessments. In the recent work, Shi et al reported the importance of ramp rate and frequency effects of a

temperature cycle in fatigue lives prediction [6]. In their work, the results were obtained based on bulk specimen of solder instead of solder joints. With the newly developed frequency-modified low cycle fatigue relationship, Shi et al's model is able to give a correct prediction in the trends of flip-chip solder joints fatigue lives undergoing thermal cycling and thermal shock tests [7,8]. However similar trend has yet to be established for BGA solder interconnects. It is thus worthwhile to examine the suitability of Shi model for BGA packages where the solder joints are much larger in size than the flip chip assemblies.

In meeting customers' requirements for faster clock speed and higher thermal performance, UTAC is in the development stage of its own High Performance flip-chip BGA package (HP-fcBGA). In this investigation, a test vehicle of size 40x40mm with 1521 pin counts (BT substrate based) is being designed. Three-dimensional (3D) finite element models are created for parametric study on stress and warpage performance, and the evaluation of solder joints fatigue life predictions. Structural analysis and comparison between the two different lid designs, materials and lid wall width have been performed. In addition, the influence of bond pad structure, die size, substrate and PCB thickness on solder joints reliability are being analyzed. Finally, fatigue lives computed by Darveaux and Shi models would be compared.

2. Package Configurations and Test Conditions

A HP-fcBGA package (BT substrate based) of size 40x40mm is being built for the study. Fig. 2 shows the schematic diagram of the package. The one-piece heat spreader made of copper graphite (CuC, CTE equals 15ppm/^{o}C) is chosen for package characterization and test measurements in this work. The lid wall width equals 4mm. The package consists of a full array pin count of 1521 (39 x 39 rows), with a solder ball diameter of 0.6mm and a pitch of 1.0mm. After the flip chip assembly process, thermal grease is applied on the top of the silicon die for providing good thermal interface with the heat spreader. Structural adhesive is then dispensed in a L-shape form at two diagonal corners of the substrate for the adhesion of the heat spreader. Finally, the package would be subjected to a reflow temperature at 150^{o}C for the curing of the adhesive before solder ball mounting. The near eutectic solder balls are used in the package.

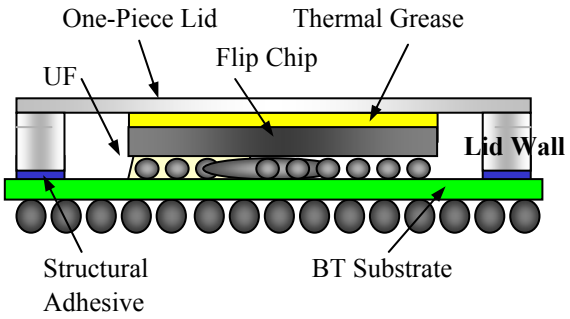


Fig 2. Schematic Diagram of a One Lid HP-fcBGA Package.

In order to study the solder joint fatigue performance, the HP-fcBGA package would be mounted onto a daisy chain FR4-PCB and subjected to two temperature cycling conditions (IPC-SM-785) as described in Table 1. The first test condition is defined as a Thermal Cycling (TC) test with a ramp rate of less than 20^{o}C/min. With a ramp rate of higher than 30^{o}C/min, the second test is being termed as a Thermal Shock (TS) test. The dwell time is 15 minutes and 10 minutes for TC and TS test respectively. The resistance of the solder interconnections is monitored continuously with an Agilent 34970A datalogger. The criteria for solder joints failure is set at a resistance change of more than 300 ohms. In order to achieve maximum package fatigue life, both the pad openings (package and PCB) are kept constant with a diameter of 0.53mm. The package bond pad design is of solder mask defined (SMD), with non-solder mask defined (NSMD) at the PCB side.

Table 1. Temperature Cycling Test Conditions.

	Test Type	Low Dwell (^{o}C)	High Dwell (^{o}C)	Ramp Time (min)	Ramp Rate (^{o}C/min)	Freq. ($1e^{-4}s^{-1}$)
1	TC	-40	+125	15	11	2.778
2	TS	-40	+125	5	33	5.556

3. Finite Element Modeling

Three-dimensional (3D) FEA models of the HP-fcBGA package were employed to simulate the physic of material deformation undergoing temperature excursion. Two finite element models namely 3D quarter and 3D slice models were created using *ANSYS 6.0* for stress and warpage analysis and solder joint fatigue lives prediction respectively (as shown in Fig. 3). The 3D quarter model was formed with the cut-out along section A-O-B, while the 3D slice represented the section O-C (Fig. 3). The first level of flip chip interconnects (solder bumps) was assumed to exhibit the behavior of the underfill layer, hence not included in both the FE models. Although only the one-piece lid HP-fcBGA package is being fabricated, the two-piece lid package would be simulated for the understanding of varying stress levels generated by different lid types. In Fig. 4a, the one-piece heat spreader is mounted onto the BT substrate by dispensing a layer of structural adhesive. On the other hand with the two-piece heat spreader, the stiffener ring acts as an interface between the substrate and the top lid heat spreader (refer to Fig 4b).

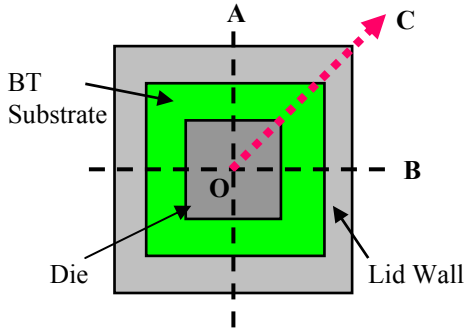


Fig 3. Package Cut-out for the 3D Quarter and 3D Slice Models.

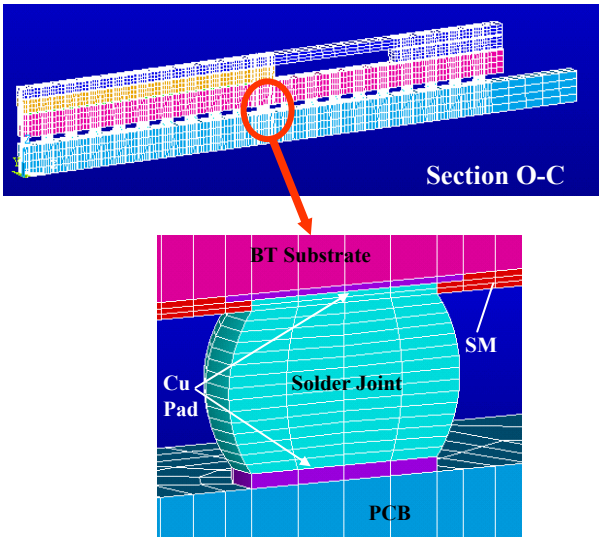


Fig 3 (cont'd). Package Cut-out for the 3D Quarter and 3D Slice Models.

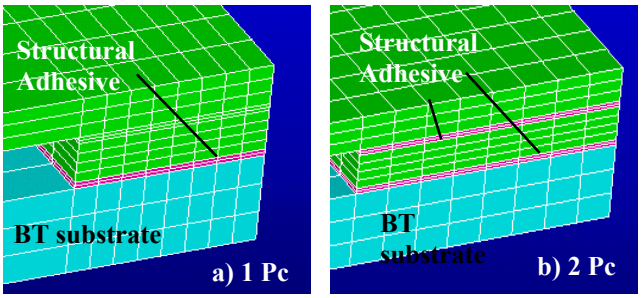


Fig 4. One Pc versus Two Pc Heat Spreader Build Up.

Table 2. Material Properties and Dimensions of the HP-fcBGA Package.

Material	E (MPa)	CTE (ppm/°C)	Poisson's Ratio	Thickness (mm)
Solder Ball	Shi's Model [11]	21	0.35	0.38 (standoff)
Cu Pad	117000	17	0.35	0.015 (Sub) 0.035 (PCB)
SM	3500	60	0.35	0.04
Die	128000	2.3	0.28	0.7
BT Substrate	25500	16 (x) 15 (y) 60 (z)	0.37	1.2 (6 layers)
Underfill	6500	$\alpha_1 = 38$ $\alpha_2 = 125$	0.3	0.08
Structural Adhesive	7000	$\alpha_1 = 48$ $\alpha_2 = 99$	0.35	0.1
Thermal Grease	0.35	232	0.35	0.06
HS (CuC)	114000	15	0.35	0.51 (Top)
				0.74 (Wall)
PCB (FR4)	23000	15 (x,y) 50 (z)	0.18	1.6 (4 layers)

The material properties and dimensions of the HP-fcBGA package are listed in Table 2. Perfect adhesion is assumed at all material interfaces. All constituent materials with the exception of the solder balls are considered to be of linear elastic behavior. To account for the non-linear creep behavior of the solder joints, Anand's model for viscoplastic material properties [5] are prescribed using ANSYS element type of VISCO107.

For package level stress analysis, the thermal profile of cooling down from the reflow condition of 150°C to room temperature of 25°C was defined for the quarter model. Test conditions as illustrated in Table 1 was specified for the slice model separately for solder joint reliability prediction. A total of three cycles of the temperature cycles would be simulated, with the stress free state at 25°C assumed. Some differences are noted between the TC and TS test conditions. Firstly, the TC test has a slower strain rate of approximately 10^{-5} s^{-1} than the TS test of 10^{-4} s^{-1}. Secondly, the TS test has a shorter cycle time and higher cyclic frequency (due to higher ramp rate) than the TC test. Lastly, there exist some differences in the failure mechanism between the two tests. Due to the gradual temperature gradient of TC test, shear loading and failure in the solder joints occurs from an interaction of shear stresses, shear fatigue and stress relaxation. Having a large temperature gradient in the TS test, the solder joints experienced a multi-axial states of stress that are dominated by tensile stress and tensile fatigue. As a result, differences in fatigue lives of the solder joints under these two tests would be expected. Previous experiments conducted [9,10] showed the influence of strain rate on the material behavior of solder under loading and at elevated temperatures. Shi et al [11] carried out some tests recently to study the effect of strain rate on the mechanical properties of the eutectic solder. It was found that the Young Modulus and yield stress are both temperature and strain rate dependent, as defined by Equations 1 and 2. Earlier study has shown that strain rate of the TC and TS test falls in the region of 10^{-5} s^{-1} and 10^{-4} s^{-1} respectively.

$$E = [(-0.006T + 4.72) * \log \dot{\varepsilon}] + (-0.117T + 37) \qquad (1)$$

$$\sigma_y = \begin{cases} (-0.22T + 62) * \dot{\varepsilon}^{(8.27e-5xT+0.0726)}, & for\ \dot{\varepsilon} \geq 5e^{-4}s^{-1} \\ (0.723 + 105.22) * \dot{\varepsilon}^{(1.6224e-3xT+0.1304)}, & for\ \dot{\varepsilon} < 5e^{-4}s^{-1} \end{cases} \qquad (2)$$

X and Y axes boundary conditions (BC) are set to describe the symmetry planes of the HP-fcBGA package. A third boundary condition, z = 0, is set at the bottom corner to prevent free rotation in space of the package during simulation. In addition, the "coupling" BCs are implemented on the slice model to account for constant nodal displacement on the coupled surfaces. Due to the different CTE properties of the constituent materials, the HP-fcBGA package will be subjected to thermally induced stresses and strains in the event of temperature excursions. High stresses would be experienced at the interfaces between constituent materials. The interfaces between the solder joint to the BT substrate and the FR4-PCB are regions of high strain concentration which are severely weakened by the inelastic strains accumulated over each thermal cycle. The solder joints and all constituent materials are subjected to a complex state of

multi-axial stress response during temperature change and thus the equivalent stress-strain concept is employed to represent the equivalent states of stress and strain in the package. The *equivalent stress* output by the finite element solver code is given by:

$$\sigma^e = \frac{1}{\sqrt{2}}[(\sigma_{xx}-\sigma_{yy})^2+(\sigma_{yy}-\sigma_{zz})^2 + (\sigma_{zz}-\sigma_{xx})^2+6(\tau_{xy}{}^2+\tau_{yz}{}^2+\tau_{xz}{}^2)]^{1/2} \quad (3)$$

where the subscripts *xx, yy,* and *zz* represent the normal components and *xy, yz* and *xz* represent the shear components.

4. Solder Joint Fatigue Life Prediction Models

The widely accepted Darveaux's volume average strain energy density model would be used to compute solder joint fatigue lives of the HP-fcBGA packages [5]. Darveaux characterized the complete failure of a solder joint into two stages: crack initiation (N_o) and crack propagation (N_a), where the life to crack initiation and the linear crack growth rate (da/dN) are given by the following expressions;

$$N_0 = K_1 \Delta W_{ave}{}^{K_2} \quad (4)$$

$$\frac{da}{dN} = K_3 \Delta W_{ave}{}^{K_4} \quad (5)$$

where K_1, K_2, K_3 and K_4 are constants for a 3D slice model that are element thickness dependent. The strain energy density, ΔW_{ave} is averaged across the elements along the solder joint interface where the crack propagates. And the fatigue life to complete failure is given by (where ϕ is the diameter of the solder joint);

$$N_f = N_o + \frac{\phi}{da/dN} \quad (6)$$

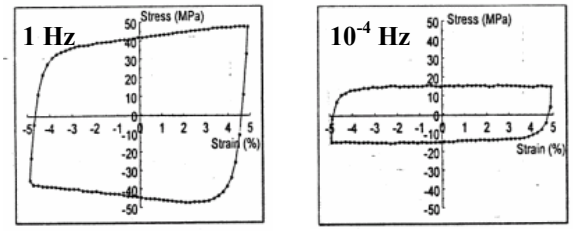
Recently, Shi et al [6] came out with a temperature and frequency dependent energy based fatigue model using the Morrow [12] energy model:

$$N_f{}^m \Delta W = C \quad (7)$$

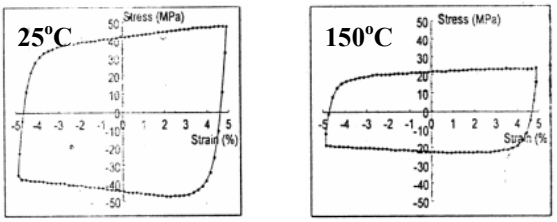
It was discovered that at a certain total strain and temperature, the area of the hysteresis loop decreased with decreasing frequency (see Fig. 5a). With another fixed total strain and frequency, the loop area decreased with increasing temperature (Fig. 5b). These evidences showed that the prediction of fatigue lives using strain energy density depends greatly on frequency and temperature. With the observations, Shi et al introduced the new frequency-modified energy based relation;

$$N_f = \left[\frac{C\Delta\sigma}{\Delta W_{nodal}}\right]^{\frac{1}{m}} \nu^{1-k} \quad (8)$$

where $\Delta\sigma$ is the stress range, ν is the frequency of the test, and C, m & k are constants that are temperature dependent. In using Shi's model, the strain energy density is based on nodal extraction rather than volume averaging as presented by Darveaux. The model has also generated close correlation in the predicted fatigue life with experimental data for a 256 I/O PBGA [13].



a) Frequency Effect (strain range 10%, temp 25°C).



b) Temperature Effect (strain range 10%, freq. 1 Hz).

Fig 5. Hysteresis Loops Obtained with Different Frequencies and Temperatures [6].

5. Results and Discussion

The HP-fcBGA model was subjected to different temperature loading for the study of package level stresses and board level solder joint reliability.

5.1. Package Type – One-Piece versus Two-Piece Lid

In this study, the 3D quarter model was used to simulate the package deformation mode. The width of the lid wall plays a critical role in ensuring good adhesion of the lid to the substrate, lowering package warpage and better assembly process control. Hence its parametric effects would be investigated in conjunction with the comparative analysis for one-piece and two-piece heat spreaders. Fig. 6 shows the warpage contour plots after cooling from the curing temperature (150°C) to ambient condition. The one-piece lid package bends downwards generally, with maximum substrate warpage at the corner of the package. While in the two-piece lid package, the portion between the lid wall and die experienced the largest warpage. The one-piece lid package has generated warpage of approximately three to four times of the two-piece type. And a longer width of the lid wall resulted in a lower warpage.

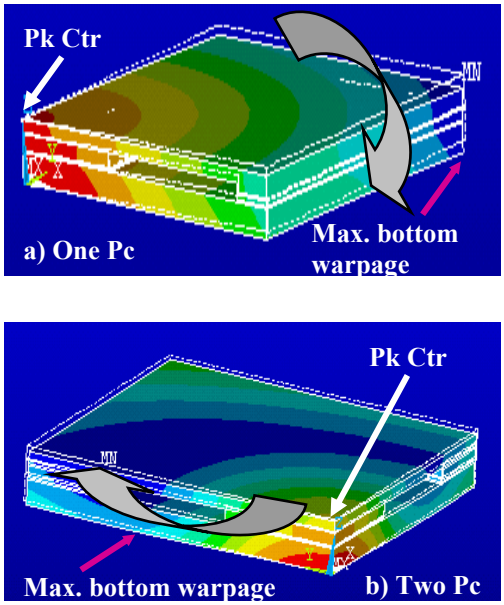


Fig 6. Package Warpage (from 150°C to 25°C).

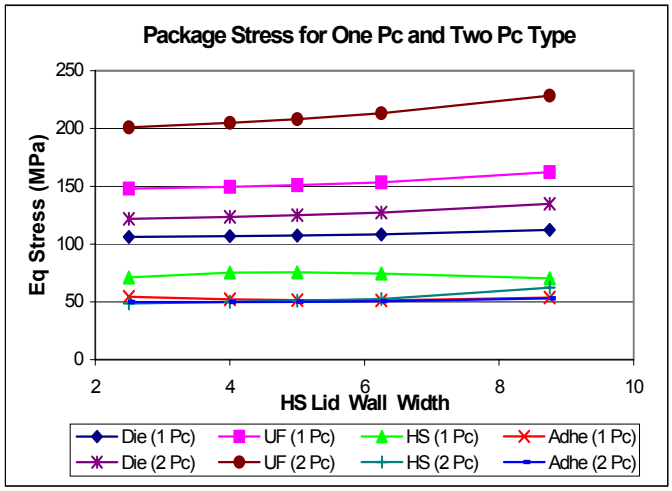


Fig 7. Package Stresses for Different Lid Types.

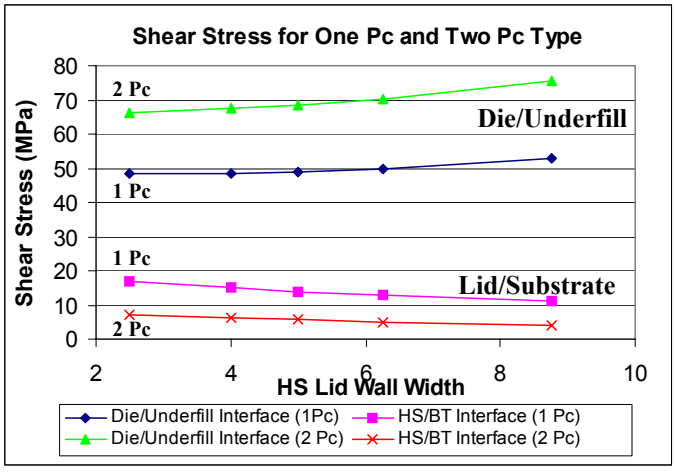


Fig 8. Shear Stresses for Different Lid Types.

The stresses in the package were analyzed next. Fig. 7 illustrates the package stresses for silicon die, underfill layer, heat spreader and structural adhesives. Slight influence of the width of lid wall was found on the one-piece type (< 10%). In the opposite, the two-piece type is more sensitive to the change in width (10% to 28% variation); a longer wall width would constitute to higher package stresses. The shear stresses at the interfaces of die/underfill and lid/substrate are illustrated in Fig. 8, where it is a measure of the adhesion strength between interface materials. It was found that the increase in width of the lid wall causes a great decrease in the shear stress at the lid/substrate interface (in both lid types). A longer lid wall provides better adhesion of the lid to the substrate. On the other hand, the width increase has resulted in an increase of the shear stress at the die/underfill interface. This is explainable because the lid wall becomes closer to the die edge as its width increases, thus creating a more interfering effect with the die and underfill. In overall, the one-piece lid package has generated lower package stresses than the two-piece type.

5.2. Solder Joint Reliability

The 3D slice model has been employed to study the HP-fcBGA package's solder joint fatigue performance. A global-local approach is being used for the analysis. To shorten the computation time and memory space, a coarse mesh of the global slice model (without details of copper bond pads and solder mask) was first constructed. The most critical solder joint location was determined to be directly under the die (due to local CTE mismatch). Detailed meshing of the solder ball (element thickness corresponds with recommended value provided by Darveaux [5]) with copper pads and solder mask were then incorporated to the critical solder joint for proper extraction of the strain energy density. With the completion of three thermal cycles, the maximum plastic strain energy was found to be accumulated in solder joint directly under the die, along the substrate side (refer to Fig. 9) and hence most susceptible to solder joint crack. The volume averaging method was thus employed at the joint interface. The effects of temperature ramp rates, package lid type, die size, substrate/PCB thickness and bond pad structure were investigated. Fatigue lives computed by Darveaux and Shi models were being compared also.

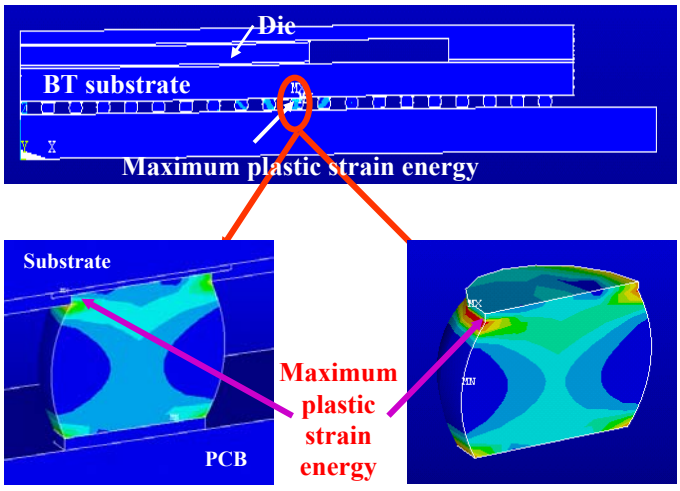


Fig 9. Maximum Strain Energy in the Solder Joint.

5.2.1. Fatigue Life Models Comparison

The test vehicles of one-piece lid HP-fcBGA would be subjected to temperature cycling tests described earlier (20 units for each TC & TS profile). Fatigue lives computed by Darveaux and Shi et al models would be correlated once the experimental data is available. Table 3 gives the fatigue lives predicted for the package undergoing TC and TS tests. Using Darveaux's model, solder joint reliability exceeded the requirements of 900 and 720 cycles for TC and TS test respectively. And a higher fatigue life was achieved by the TC test than the TS test. Similar trend has been observed by other studies on BGA packages [2,14]. On the other hand, an opposite trend was obtained while using Shi et al frequency-modified life equation. With the dependency of the stress range and frequency effect, Shi et al's prediction was more conservative for the TC test but closer to Darveaux model's prediction for the TS test. And it has computed a higher fatigue life of the TS than the TC test. Shi has showed good correlation between predicted life with experimental data in his subsequent work [13]. The trend of a higher TS fatigue life compared to a TC test could also be found in other investigations on flip chip solder bumps [15,16], though not BGA solder joints. With no experimental data existing at the present moment, it would be difficult to conclude any inaccuracy in Shi et al model. As a result, further analysis would be required to understand this phenomena. With the correct trend of fatigue life predicted, Darveaux's model would be used for subsequent computations.

Table 3. Fatigue Lives Predictions for HP-fcBGA Package.

Test Type	Fatigue Life Model		Req'd (cycles)	Freq. ($1e^{-4}s^{-1}$)	Ramp Rate (°C/min)
	Darveaux [5]	Shi et al [6]			
Thermal Cycling	939 cycles	545 cycles	900	2.778	11
Thermal Shock	799 cycles	737 cycles	720	5.556	33

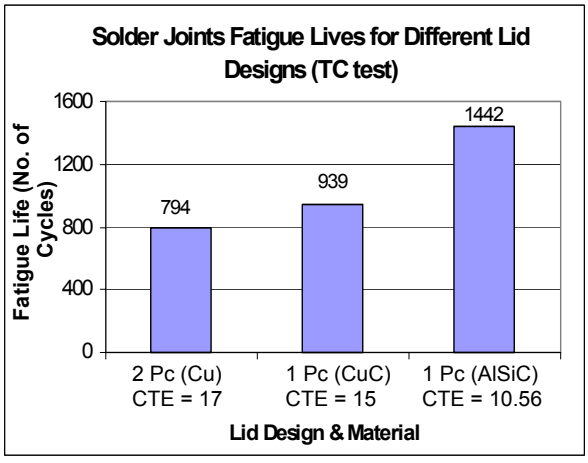


Fig 10. Solder Joint Fatigue Life for Lid Type and Material Comparison.

5.2.2. One-Piece versus Two-Piece Lid

The impact of lid materials and types on the solder joint reliability undergoing TC test has been studied. Fig 10 shows that the two-piece lid package with base material of copper has generated a lowest fatigue life, while a higher fatigue life could be achieved by using the AlSiC one-piece type. A lower value in CTE of the heat spreader has constituted to a higher fatigue life of the solder joints. The reason can be attributed to a smaller CTE mismatch with the silicon die, hence reducing the stress transmitted to the solder joints.

5.2.3. Structural Parametric Effects

Parametric studies have been performed on die size, substrate and PCB thickness, and PCB bond pad structure for the one-piece lid package. The variations in the above parameters are essential in meeting different customer applications and requirements, for instances thinner overall package height and different PCB used by end users. Fig.11 reflects the variation in solder joint fatigue lives for die size, substrate and PCB thickness. It could be seen that longer fatigue life could be obtained for a smaller die. Since the critical solder joint is located directly under the die edge, a smaller die size would constitute to a smaller DNP (distance from neutral point) and thus generating higher fatigue life. A decrease in the substrate thickness has resulted in the increment of the fatigue lives. The reason can be attributed to the reduction in global CTE mismatch with the PCB, hence improving the fatigue performance of the interconnects. Solder joint reliability is observed to be most sensitive to the variation in PCB thickness. In reducing the overall assembly bending with a thicker PCB, it helps in lowering the chances of solder joint cracks. Lastly, finite element simulation showed that with the change of the NSMD bond pad on the PCB to a SMD structure, only slight variation in the solder joint fatigue life was observed. And the crack initiation region remains at the joint to substrate interface. Hence other parameters such as pad size variations, solder mask opening and solder standoff height can be further investigated for joint reliability enhancement.

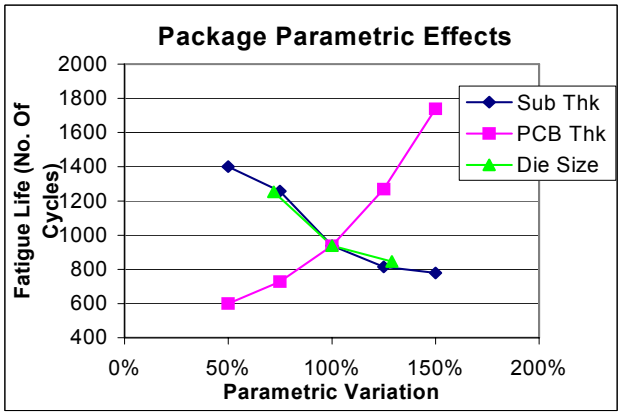


Fig 11. Package Parametric Effect on Solder Joint Reliability.

6. Conclusions

Reliability assessments of the HP-fcBGA package at both the package and board levels utilizing FEA have been completed. The conclusions drawn in the study includes:

- The one-piece design has generated lower package stress than the two-piece type. On the other hand, the high warpage resulted after adhesive curing might pose a concern for board assembly process. However this concern could be overcome by increasing the width of the lid wall. Due to the higher material and assembly cost incurred for the two-piece type, the one-piece design offers a potential choice for lower induced package stresses.
- The use of Darveaux and Shi et al models has revealed different trends of fatigue lives predicted for the TC and TS tests. Validation in the trends would be conducted with the actual experimental life data.
- The one-piece package has resulted in a higher fatigue performance of the solder interconnects. Parametric studies found that solder joints reliability can be enhanced by a decrement in the die size and substrate thickness, and is achievable using a thicker PCB.

The findings would be useful for UTAC's continuous effort in developing its high performance flip chip BGA packages.

7. Future Work

Correlation of predicted fatigue lives with experimental data would be performed. The trend of fatigue lives for TC/TS computed using Shi' model would be further investigated.

Acknowledgments

The authors would like to thank the Flip Chip development group of UTAC for their support in the sample build of the test vehicles and the valuable discussions in the package assembly processes. The use of thermal chamber and measurement systems in the Nanyang Technological University (Singapore) is also greatly appreciated.

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