GaN PACKAGES' PERFORMANCE STUDY UTILIZING FEM ANALYSIS AND ACTUAL ASSEMBLY BUILD FOR VALIDATION

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ABSTRACT

Gallium nitride (GaN) devices have been widely used for military radar and LED lighting applications owing to superior power density/ efficiency, providing more than 2X the power output of other semiconductor devices (i.e. Si) with unique ability for high frequency fast switching speeds. Over the past few years significant cost reductions have been achieved in GaN wafer fabrication, allowing a range of commercial applications to achieve energy savings, size and weight reductions in power supply modules. Servers, 4G wireless base-stations, LED TVs, automotive and industrial motors are all looking to GaN devices for energy and size reduction requirements.

Wide bandgap, high-electron mobility and saturated electron velocity performance advantages with GaN devices becomes a market driver since defense and commercial applications continue to push power and bandwidth limitations. Market research firms project that GaN power devices will approach $600M in 2020, consuming 580,000 (6" equivalent) wafers and ramp-up significantly over the next 5 years [1][2]. GaN is still more costly than Si, however GaN based power supplies reduce energy costs and if pricing matches Si equivalents devices GaN adoption will spread in consumer applications.

As we see the trend in terms of power management direction and the need for higher frequency application, a study to understand GaN devices in terms of overall packaging were performed. Unlike conventional Si based packages, GaN packages are attractive for high power, high frequency capabilities which required operating at high temperature. Thermal management is crucial for low thermal resistance, high power density compatibility and long term reliability. High thermal conductive die attach solder with high peak reflow temperature poses risk on die crack during assembly due to thermo-mechanical stress. Signal and Power integrity, low parasitic and cross-talk analysis is essentials to ensure good performance in high frequency range.

Finite element modeling (FEM) and Computational Fluid Dynamics (CFD) based Thermal, Mechanical and Electrical simulation analysis are being performed to characterize the performance and reliability of the GaN, GaN on SIC, Si, SIC packages. Various packaging materials and structure will be studied with Ansys Static Structural analysis for enhanced compliance between chip and package to mitigate risks that would arise during assembly and device operation. Quad flat no lead (QFN) package exposed die attached paddle enables direct thermal path from chip to PCB for efficient heat dissipation, excellent thermal performance and high power usage. GaN devices are proven to be reliable at high junction temperature as high as 225°C. CFD analysis is done on GaN in QFN package for enhanced

thermal performance. For wideband performance and high frequency application package, electrical performance is constraint by chip to package parasitic. Electrical simulation is carried out for parasitic extraction and signal integrity. Actual assembly build and assessment are conducted to validate the FEM analysis findings.

REFERENCES

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