3D SiP with Embedded Chip Providing Integration Solutions for Power Applications

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INTRODUCTION

Multi-chip and system in a package (SiP) technologies are seeing strong demand across a range of applications, providing heterogeneous integration benefits enabled by expanding supply chains. Design requirements for higher levels of integration and performance in smaller form factors drive the need for 3D package architectures. Die and package stacking technologies are the basis of most 3D package architectures. These technologies serve memory and logic device stacking requirements well, however, power electronics applications require higher power and thermal performance levels. 3D SiP with embedded chip technologies are emerging as a leading architecture for power integration requirements. This paper will summarize examples of 3D SiP with embedded chip solutions and address new supply chain developments.

DEFINITIONS

Multi-chip package (MCP) - integrates two or more ICs in a standard package platform. The platform can utilize lead frame, laminate, ceramic based substrates or wafer level processing and can be in a planar (2D) or stacked (3D) architecture. Typically passives are not integrated but the trend is for increased use of a few passives for signal conditioning of MCPs at higher frequencies or performance.

System in a package (SiP) – provides heterogeneous integration of ICs with passive components into a standard package platform to provide sub-system optimized performance as a functional block. SiP designs have shorter time to market and much lower NRE costs vs. a SoC.

Modules – are best characterized as custom integrated assembly solutions designed for specific functions within a system and typically require a connector or flex circuit interface to the main printed circuit board assembly (PCBA). Whereas MCP and SiP solutions are mounted on a PCBA using standard SMT processes.

Table 1 (1) provides a forecast by Prismark of SiP and MCP product / package types and leading supply chain providers.

SiP/MCP FORECAST

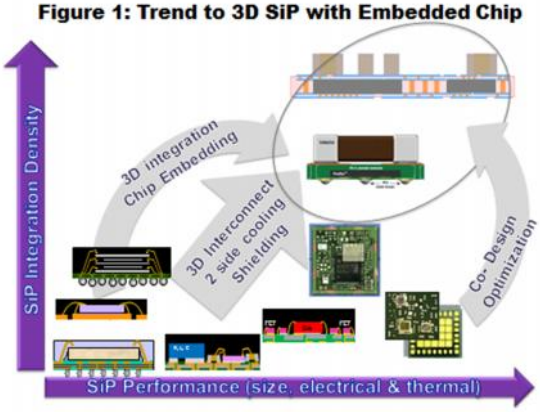
Product/Package Type Volume (Bn Units)	2014	2019F	Leading Suppliers/Players
Stacked Die In Package and Memory Card	8.3	10.5	Samsung, Micron, SKHynix, Toshiba, SanDisk PTI, ASE, SPIL, Amkor, STATS ChipPAC
Stacked Package on Package: Bottom Package Only	0.95	1.2	Samsung, Apple, Qualcomm, Mediatek Amkor, STATS ChipPAC, ASE, SPIL
PA Centric RF Module	4.5	5.9	Qorvo, Skyworks, Anadigics, Avago, Amkor, ASE, Inari, HEG, JCET. Unisem, ShunSin
Connectivity Module (Bluetooth/WLAN)	0.5	0.7	Murata, Taiyo Yuden, Samsung, ACSIP, ALPS, USI
Graphics/CPU or ASIC MCP	0.25	0.20	Intel, AMD, Nvidia, Xilinx, Altera
Leadframe Module (Power/Other)	3.2	4.7	NXP, STMicro, TI, Freescale, Toshiba, Infineon/IR, Renesas, ON Semi
MEMS and Controller	5.4	8.2	ST, Analog, Bosch, Freescale, Knowles, InvenSense, Denso
Total	**23.1**	**31.4**	

Estimating and forecasting total annual shipments of SiP, MCP, or modules along with segmenting by package type or architecture has been a challenge for industry analysts. Not only are a diverse range of hard to classify new

package types emerging but many suppliers have different definitions of a SiP vs MCP or have legacy accounting systems that make it hard to capture and segment by assembly architecture including 3D / stacking. What analysts can agree on is that economic and time-to-market forces are favoring package integration solutions over SoC designs. Further, 3D architectural benefits will lead to growth in 3D stacking across many applications and package types. A conservative estimate is that over 10 billion 3D packages shipped in 2014 with growth projections to over 20 billion by 2019 for a 15% CAGR. Many of these 3D package solutions will have SiP integration and performance attributes.

3D SiP with embedded chip technology has integration, performance and 3D architecture flexibility that can offer benefits to a wide range of applications. 3D SiP with embedded chip typically requires wafer level, substrate fabrication, microelectronic and SMT process technologies which to date has been a limitation for turnkey supply chain solutions. **Figure 1** (2) illustrates the trend to 3D SiP and the integration density and performance benefits enabled by embedded chip technology.

Figure 1: Trend to 3D SiP with Embedded Chip



The following is a list of performance advantages (+) and trade-offs (-) for 3D SiP with embedded chip vs. traditional planar (2D) SiP assembly technologies.

- Miniaturization:

  + Reduced SiP component footprint area
  - Increased SiP component mounted Z height
- Design flexibility:

  + Ability to tailor the interconnect technology (embedded via, wirebond, FC or SMT) best suited for the IC or passive device requirements being integrated. This allows embedded chip technology to provide higher wiring density solutions.
  - A co-design methodology is required to optimize for system and device cost / performance trade-offs.
  - Chips first assembly technologies like substrate or fan-out wafer level package (FO-WLP) embedding, require closer co-design relationships to address KGD requirements, design for test & yield optimization.
- Electrical performance:

  + Improved signal integrity or power efficiency thru shorter vertical (via) interconnects, power / ground planes in embedded chip substrates and lower package parasitics.

  + EMI / RFI shielding and isolation of digital and RF devices thru ground planes and plated via based ground fences along with the ability to shield the top side assembly thru as shield cap or conformal shield layer over a mold cap.

  + 3D SiP architecture enables closer placement of critical passives (inductors, capacitors, filters, etc…) to IC devices.

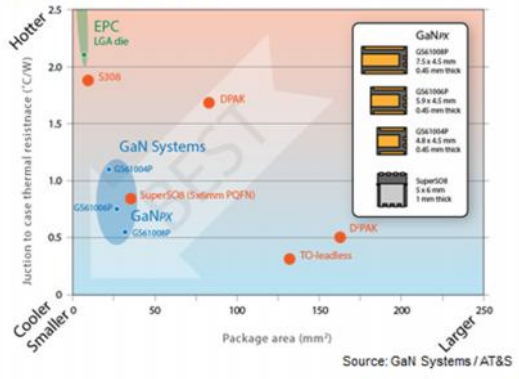
- Thermal performance:

  + Integrated heat spreading copper layers within embedded chip substrate offering lower thermal resistances.

  + Ability for two sided cooling and ease of chip hot spot thermal management.

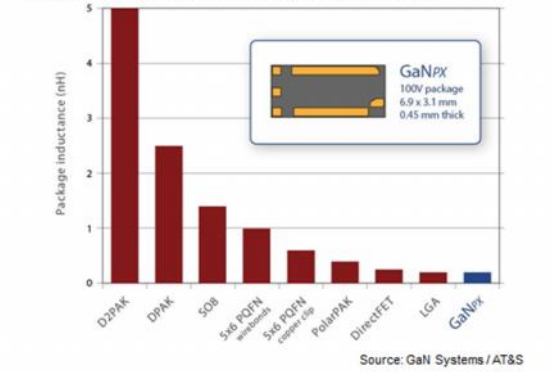
Miniaturization and thermal benefits were reported in **Figure 2** (3) where GaN System and AT&S provide a comparison of package area vs thermal resistance. The GaNpx embedded chip in substrate solutions (ranging from 33.75 to 21.6 sq. mm) can provide a smaller and cooler performing package vs. a range of assembly based power package options. Only the 5x6mm PQFN (with Cu clip) achieves similar size and thermal resistance performance. In all cases the actual thermal performance is impacted by the chip size and substrate or leadframe thicknesses, so the package rank positions are an approximation.

Figure 2: Comparison of Package Area vs. Thermal Resistance



Further, GaN Systems and AT&S reported electrical benefits in **Figure 3** (3) positioning these same power package solutions by their drive loop and cumulative circuit path as a package (connection) inductance ranking. The power package options that utilize direct bond interconnect (low inductance flip chip or plated contacts via embedded chip technology) offer the lowest package inductance.

Figure 3: Package Inductance Ranking



Due to these thermal, electrical and small package size benefits, the industry is seeing the emergence of embedded chip in substrate technology for power management applications from **Figure 4** TI's MicroSiP™ and MicroSiL (4, 5), Infineon's DrBlade™ (6) to the emerging Heterogeneously Integrated Power Stages (HIPS) technology offered by Sarda Technologies (7) which like TI's solutions relies on a true 3D SiP with embedded chip technology architecture as shown in **Figure 5**.

Figure 4: TI MicroSiP™

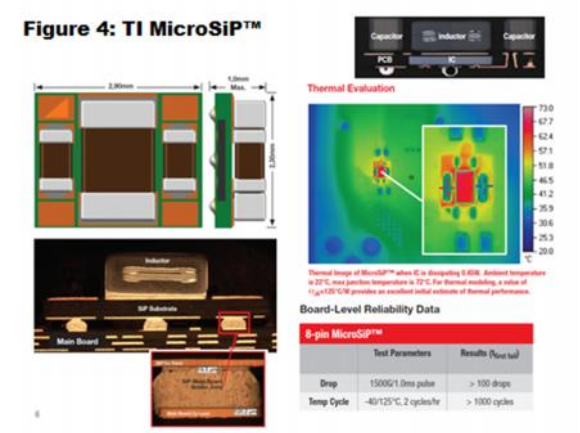
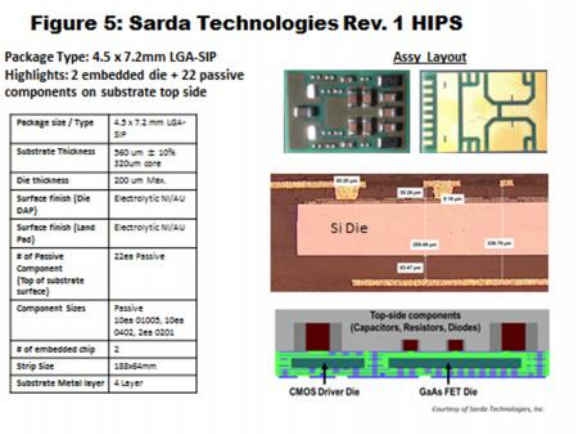
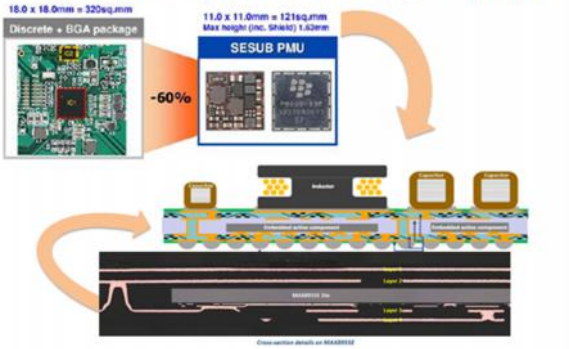


Figure 5: Sarda Technologies Rev. 1 HIPS



To date one of the highest levels of integration in a 3D SiP with embedded chip application can be seen in **Figure 6**. Here Research in Motion worked with TDK to shrink the power management section of a BlackBerry™ Z10 smartphone by 60% by embedding 2 Maxim chips in TDK's SESUB (Semiconductor Embedded in SUBstrate) technology and surface mounting 34 passives on the top side under a RF shield cap. (8,9)

Figure 6: TDK's SESUB Technology shrinks Power Management section 60% in BlackBerry™ Z10 Phone



Recently, Intel announced their EMIB (Embedded Multi-die Interconnect Bridge) technology as solution for high bandwidth memory to logic chip integration by embedding an interconnect bridge chip in a high density build up substrate to handle the high wiring density. In Intel's applications a 2.5D package architecture with a TSV based silicon interposer has been the incumbent technology of choice. **Table 2**, summarizes Intel's attributes evaluation matrix favoring EMIB over a silicon interposer based 2.5D package architecture (10, 11). As the yellow bar indicates a key development focus for Intel was in the embedded die in substrate processing which was completed in collaboration with substrate fabrication partners. A co-design methodology is required beginning at the device floor planning stage for both the memory and logic die, to optimize the memory interface for connection thru the substrate and embedded bridge chip.

Table 2: EMIB vs. 2.5D Silicon Interposer: Evaluation Matrix

	Silicon Interposer	EMIB
Wiring Density		
Chip-to-Chip Signal Integrity		
Through Package Signal Integrity		
Through Package Power Delivery		
Silicon Processing		
Substrate Processing		
Assembly Processing		
Total Chip/SI Area on Package		
Overall Cost		
Final Recommendation		☑

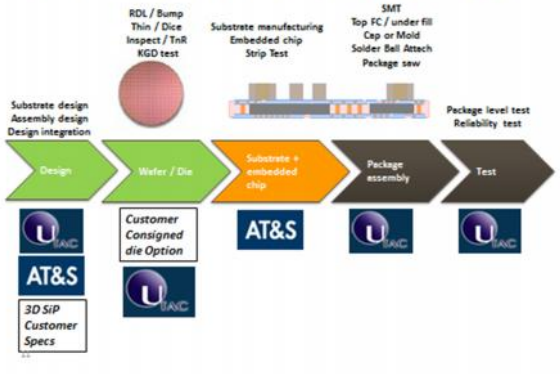
Source: Intel Corp. R. Mahajan keynote IMAPS DPC 2016

By applying the form factor and performance benefits 3D SiP with embedded chip offers. Against the package attributes required for next generation RF PA, Connectivity and other SiP applications; system, IC and package designers can envision the benefits available from a 3D vs a planar SiP architecture. **Figure 7** (12) illustrates the applications and device integration available through 3D SiP with embedded chip technologies. Embedded chip in substrate market leaders AT&S and TDK have been serving power and wireless applications in high volume manufacturing for a number of years.

Figure 7: Applications for 3D SiP with Embedded chip

With a widening range of applications representing strong demand for 3D SiP with embedded chip technologies, coupled with the co-design and process technology complexities associate, the supply chain could become a serious constraint to the technology's adoption. Very few worldwide suppliers have the resources and depth of technologies to provide a vertically integrated supply chain solution. To address this constraint, apply industry leading capabilities in embedded chip substrates, wafer level and SiP assembly technologies - AT&S and UTAC Group entered into a joint marketing collaboration agreement in April of 2015. This collaboration is providing virtual turnkey supply chain options to the market with provisions for either AT&S or UTAC to directly serve customers. **Figure 8** (2,13) illustrates the business and supply chain flow offered by the AT&S and UTAC collaboration. Over the past year design rules and roadmaps have been aligned and a 3D SiP test vehicle has been fabricated delivered to Alpha customer Sarda Technologies.

Figure 8: Collaborative 3D SiP Supply Chain Flow



3D SiP with Embedded Chip Reliability

The AT&S embedded chip in substrate technology has met JEDEC long term package reliability requirements, with customers performing their own reliability qualification testing. **Table 3**, summarizes the testing AT&S has completed along with UTAC's reliability requirements for laminated based packages. UTAC and AT&S are teaming to create additional reliability data for sharing with customers as required.

Table 3: 3D SiP w/ Embedded Chip Reliability

AT&S 4L 120x120mm TV 0.9x0.9 & 5.9x5.9mm embedded die			UTAC Laminate Req't
Method	Specification	Result	Specification
Moisture Sensitivity Level	Peak @ 260 C	Minimum MSL3	MSL3
Thermal Cycling	-55 C / +150 C	1000cycles passed (TC Grade 1)	-55 C / +125 C ; 1000 cycles
HAST	110 C @ 85%RH @ 5VDC	264 hours passed	uHAST - 130 C/85%RH; 96 hours
High Temperature Storage	@125 C	1000hours passed (TH Grade 2)	150 C ; 1000 hours
Temperature/ Humidity	85 C / 85%RH	1000hours passed (TH Group A)	Per customer
Board bending	5mm/s	80K bends passed	Per customer
Random vibration	3 g (rms) (5-500) Hz	30 min per axis passed	Per customer
Shock	10kg @ 0.2ms	3 per direction passed	Per customer
Reflow sensitivity	Pb-free profile (255 C)	30 cycles passed	Per customer
Drop Test	1500g @ 0.5ms	10 drops passed (MS Group F)	Per customer

Conclusions:

MCP and SiP applications are expanding rapidly, enabled by advances in wafer level and substrate interconnect processes. 3D SiP with embedded chip technology can provide package architecture, integration and benefits for a diverse range of applications or performance attributes required. Power management and wireless applications have been delivering 3D SiP with embedded chip solutions for nearly a decade. New 3D SiP solutions are emerging offered by a broader range of IC suppliers to leverage both performance and cost benefits. UTAC's collaboration with AT&S offers the market a full turnkey supply chain solution addressing design for cost / performance requirements to enable customers to bring 3D SiP with embedded chip products to market more efficiently.

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