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FINITE ELEMENT PARAMETRIC ANALYSIS ON FINE-PITCH BGA (FBGA) PACKAGES

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ABSTRACT

Reduction in size of portable products such as cellular phones and camcorders has led to the miniaturization of integrated circuit packages. *Fine-pitch BGA* (FBGA) packages has been gaining its popularity due to compact in size and relatively low costing. With further down-sizing in package height, reliability issues like die cracking and warpage have surfaced as potential failures. Die cracks results in malfunction of an IC package, while the latter causes difficulty in board surface mounting. In this study, effects of package height on the die stress and warpage have been assessed by FEA. With overmold height ranging from 0.4~0.6mm and substrate from 0.16~0.32mm thick, the Overall Package Thickness coding from "T" ($1.00 < A \leq 1.20$ mm) to "W" ($0.65 < A \leq 0.80$ mm) are being analyzed. Results revealed that die stress and warpage decreases with increase in overmold thickness. However, an increment in the substrate thickness constituted to a rise in die stress and warpage. It was found that "top clearance" (distance between active die side and package top) of the package contributed to different trends in die stresses. Trends of results in varying the package and die sizes are also being investigated. The findings have provided guidelines for in-house designers in containing possible failures in FBGA packages.

INTRODUCTION

With the increasing demand of smaller and thinner IC packages to meet the reduction in size of portable consumer products as such personal digital assistance (PDA), cellular

phones and digital cameras, the relative low cost and compact *fine-pitch BGA* (FBGA) packages have emerged as a popular choice. With the use of thin core substrate material and the decrease in overmold encapsulant thickness, the overall height of the FBGA package can be reduced significantly. This has called for a need from the JEDEC committee to define the Standard Overall Height Codes for these new packages. Table 1 shows the standard overall height thickness code defined [1]. The thickness codes are for the "Overall Profile ("A" Maximum) Height" and not the package body thickness alone.

Table 1. Standard overall height thickness code.

Code	Description	Overall Ht. ("A")
None	Standard Profile	$A > 1.70$ mm
L	Low Profile	$1.20 < A \leq 1.70$ mm
T	Thin Profile	$1.00 < A \leq 1.20$ mm
V	Very-Thin Profile	$0.80 < A \leq 1.00$ mm
W	Very-Very-Thin Profile	$0.65 < A \leq 0.80$ mm
U	Ultra-Thin Profile	$0.50 < A \leq 0.65$ mm
X	Extremely-Thin Profile	$A \leq 0.50$ mm

During the assembly process and reliability testing of the FBGA packages, failure issues like die cracking and excessive warpage have surfaced as potential problems. Firstly, cracking in a die will result in the malfunction of an IC circuitry, and render the package useless. With the further thinning of the silicon die to cater for low profile of the IC packages, the concern of high die stresses induced begin to surface. Secondly, chemical shrinkage of the mold compound during curing will

contribute to the warpage of a plastic encapsulated package [2,3]. In addition, due to the mismatch in CTE (coefficient of thermal expansion) between constituent materials in the subsequent cooling from post mold cure temperature (commonly of around 175°C) to room temperature, further warpage in the package is resulted. Excessive package warpage will cause great difficulty in assembly related issues such as solder ball attach and unit singulation process, and most importantly the eventual surface mounting onto PCB.

The finite element analysis (FEA) method has been employed widely to investigate the warpage behavior in plastic encapsulated packages [4,5]. Studies have shown that the use of viscoelastic model representation for mold compound has generated close predictions in the package warpage measurements. However these viscoelastic material properties are not readily available from mold compound suppliers, and time and temperature dependent viscoelastic properties have to be determined experimentally. In Tee et. al. work [4], it was found that elastic model has always predicted higher warpage than actual measurements. Nonetheless, the elastic model is able to reflect the general trend of warpage in the five cases that have been analyzed. Thus, the elastic model can be used to provide an estimation of package warpage when viscoelastic properties of mold compound are not available.

In the current work, elastic material properties are used for the modeling of the mold compound. Appropriate CTE values are defined to account for the different CTE of the mold compound over the glass transition temperature (Tg). Overall Package Thickness coding from “T” (1.00<A<=1.20mm) to “W” (0.65<A<=0.80mm) are being analyzed with variations in overmold, BT substrate and die thickness. Parametric effects of the package and die sizes are investigated as well. The trends in findings of the package warpage and die stress will provide reference design guidelines for in-house designers in containing possible failures in FBGA packages. However, other IC package failure drivers such as interfacial stresses between the die and mold compound, and other parametric effects like the content of copper traces in the BT substrate would not be addressed in this paper.

FBGA PACKAGE WARPAGE MEASUREMENTS

Warpages were measured from a particular design of the FBGA package (13x8x1.07mm, “T” thickness code) using three different types of mold compound. The measurements were taken after the packages were cooled from the post mold cure temperature (~175°C) to ambient room temperature. Multiple packages were measured for package warpage with the average data presented in Table 2. It could be seen that FBGA with mold compound ‘M1’ experienced the largest warpage. The reason can be attributed to the lowest CTE1 of ‘M1’ which resulted in a maximum mismatch with the BT substrate (CTE_{x,y} = 15ppm/°C), followed by mold compounds of ‘M2’ and ‘M3’.

The measured data would also be served as a form of validation for the finite element modeling results.

Table 2. FBGA warpage measurements for different mold compounds.

Mold Cmp	E (MPa)	CTE1	CTE2	Tg (°C)	Warpage (um)
M1	21560	8	36	130	110.4
M2	24500	10	39	155	83.4
M3	22000	11	38	185	57.5

*Units of CTE is in ppm/°C

THERMAL STRESS AND STRAIN ANALYSIS

Due to the different CTE properties of the constituent materials (silicon die, mold compound, die attach adhesive and BT substrate), the FBGA package will be subjected to thermally induced stresses and strains in the event of cooling down from the post mold cure temperature. High stresses would be experienced at the interfaces between constituent materials and result in potential failure. It is understood that the maximum principal stress is normally used for the indication of brittle materials failure. The silicon die is subjected to a complex state of multi-axial stress response during temperature excursion and thus the von Mises stress concept is employed (instead of maximum principal stress) to represent the equivalent state of stress in the die. The *von Mises stress* output by the finite element solver code is given by:

$$\sigma^e = \frac{1}{\sqrt{2}} [(\sigma_{xx} - \sigma_{yy})^2 + (\sigma_{yy} - \sigma_{zz})^2 + (\sigma_{zz} - \sigma_{xx})^2 + 6(\tau_{xy}^2 + \tau_{yz}^2 + \tau_{xz}^2)]^{1/2} \quad (1)$$

where the subscripts *xx*, *yy*, and *zz* represent the normal components and *xy*, *yz* and *xz* represent the shear components.

FINITE ELEMENT MODELING

3-dimensional (3D) FEA model of the FBGA package was created to simulate the cooling condition from post mold cure temperature to room temperature. For geometric symmetry purpose, the baseline package dimensions are taken to be 13x13mm with a die size of 10x10mm. A quarter symmetry model of the FBGA was being modeled using ANSYS 3D element type 45 (Fig. 1). A thermal loading from 175°C to 25°C was prescribed to the model, with the stress free state taken to be at 175°C. Perfect adhesion between constituent parts was also assumed in the modeling.

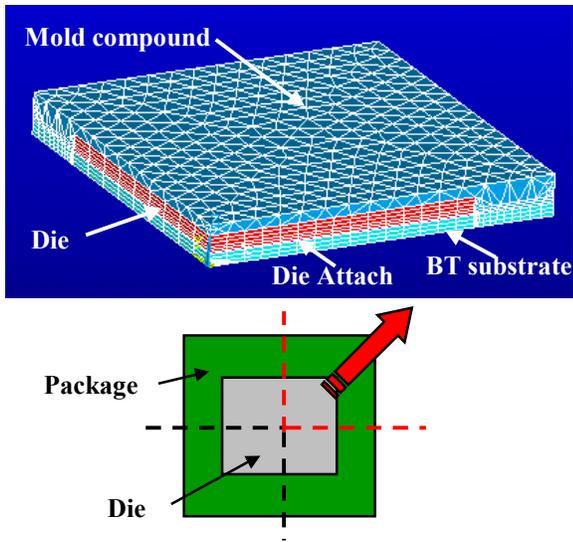


Figure 1. 3D quarter finite element model of the FBGA package.

As shown in Fig. 2, variations in die thickness (0.16, 0.18, 0.21, 0.24, 0.28, 0.3, 0.32mm), BT substrate thickness (0.16, 0.18, 0.2, 0.24, 0.28, 0.3, 0.35mm) and overmold thickness (0.4, 0.5, 0.6mm) were considered for the parametric study. The die attach material thickness equals 0.03mm. With a nominal solder ball standoff height of 0.22mm after ball attach, a minimum overall package thickness of 0.78mm (“W” code = 0.22standoff + 0.16substrate + 0.4overmold) could be achieved. Correspondingly, a maximum overall package thickness of 1.17mm (“T” code) is being obtained. The mechanical properties of all materials are taken to be homogenous and listed in Table 3. Due to the unavailability of viscoelastic properties of the mold compound, elastic properties are assumed. Appropriate CTE values are prescribed to account for the different CTE over glass transition temperature (T_g) in the die attach and mold compound materials.

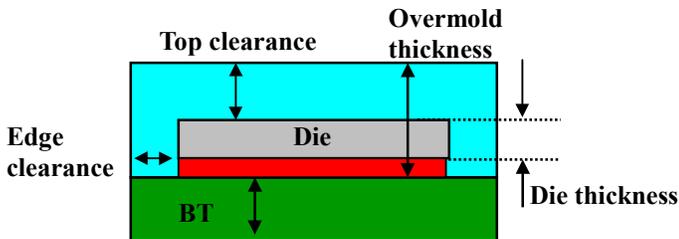


Figure 2. Schematic diagram for the FBGA package.

Table 3. Material properties of the FBGA model.

Material	E (MPa)	CTE (ppm/°C)	T _g (°C)
Mold Compound	23600	$\alpha_1 = 10$ $\alpha_2 = 37$	118
Silicon Die	128000	2.3	-
BT Substrate	25500	15 (x) 16 (y) 60 (z)	-
Die Attach	724	$\alpha_1 = 45$ $\alpha_2 = 136$	42

RESULTS AND DISCUSSION

Finite element software of *ANSYS (version 6.0)* was used to simulate the FBGA package deformation behavior. Package warpages and die stresses after post mold cure cooling were extracted for analysis.

Correlation of FEA Results with Measurement

A finite element model was first created to compare with the warpage measurements reported earlier. As shown in Fig. 3, the predicted warpages obtained by simulation were lower than the measured values. It is of opposite observation to Tee et. al. [4] findings. However, the FEA warpage agreed with the decreasing trend of the experimental data. Situations of over or under estimated values have been commonly encountered in finite element analyses. It is of importance in individuals’ judgement to use the results wisely. In cases where correlation in absolute values cannot be achieved, the trends in results obtained would still be useful for general design guidelines.

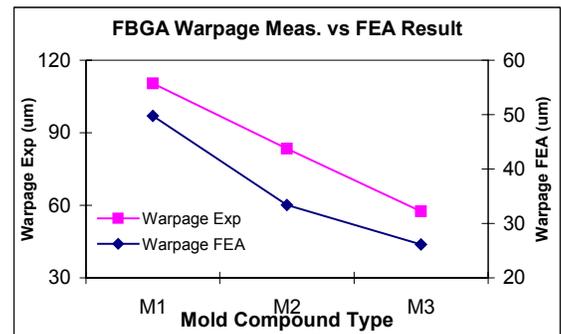


Figure 3. FBGA warpage measurements versus FEA results.

BT Substrate, Die and Overmold Thickness

The change in package height due to variations in BT substrate and overmold thickness has significant impact on the warpage and die stress. In Fig. 4, the increase in warpage with substrate and die thickness was illustrated for overmold thickness of 0.5 and 0.6mm. As either the substrate or die thickness increases, the effective CTE mismatch between the interface materials would increase. In return it constitutes to a higher warpage. Fig. 5 reveals a turning point in warpage existed with a top clearance (refer to Fig. 2) of less than 0.09mm for 0.4mm overmold. It could be anticipated that the

top clearance would have some influence on the package deformation behavior. With a maximum die thickness of 0.32mm, no turning point was observed for overmold of 0.5 and 0.6mm as the minimum top clearance exceeds 0.09mm.

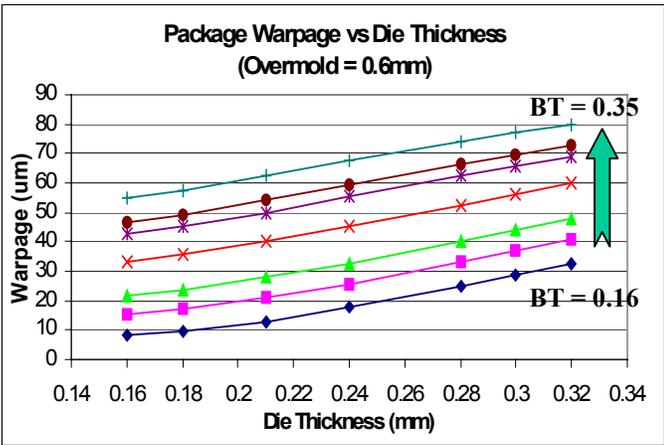
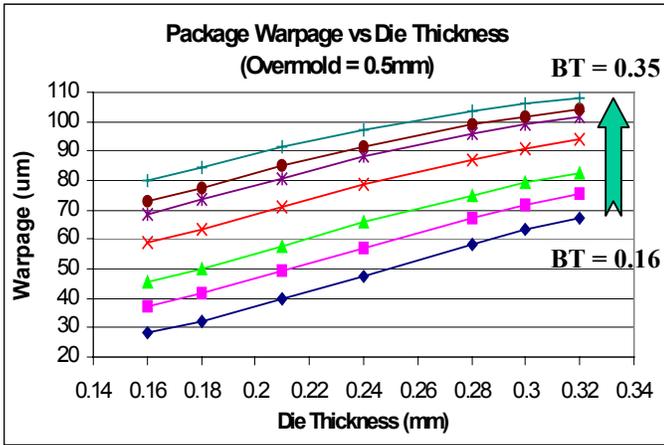


Figure 4. Trends of predicted package warpage (overmold thickness of 0.5 and 0.6mm).

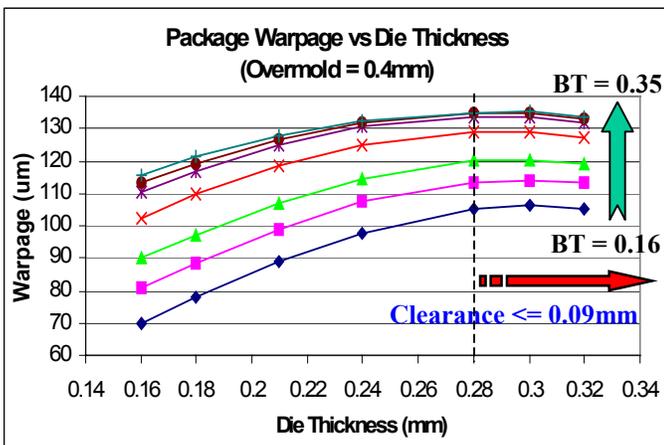


Figure 5. Trends of predicted package warpage (overmold thickness of 0.4mm).

The silicon die stress behaves quite differently from the package warpage. As shown in Fig. 6, the stress extracted from the outermost die edge (maximum stress value in most cases) decreases as the die thickness increases. The reason can be attributed to spreading of stress over a thicker die. On the other hand, a thicker substrate has generated higher die stress. As explained in the preceding discussion, package warpage increases with a thicker substrate. As a result, a higher stress is being exerted onto the die (while the die thickness remains constant). The top clearance has again revealed some effect on the die stress for thinner overmold. In Fig. 7, a turning point in die stress existed with a top clearance of less than 0.13mm (0.4mm overmold). And no turning point was observed for overmold of 0.5 and 0.6mm as the minimum top clearance exceeds 0.13mm (with maximum die thickness of 0.32mm). More detailed discussion on the effect of clearance would be presented in the subsequent section. From the magnitude of the plots in Figs. 4 to 7, both the package warpage and die stress decrease with the increase in overmold thickness.

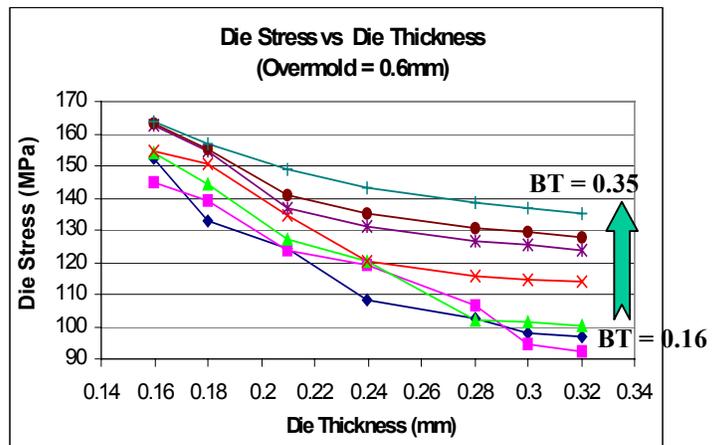
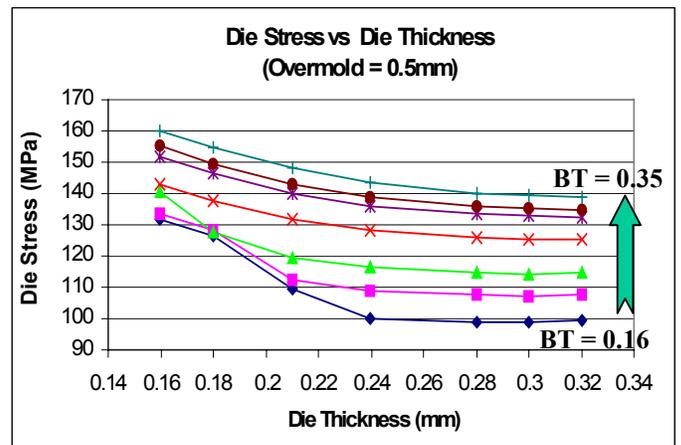


Figure 6. Trends of silicon die stress (overmold thickness of 0.5 and 0.6mm).

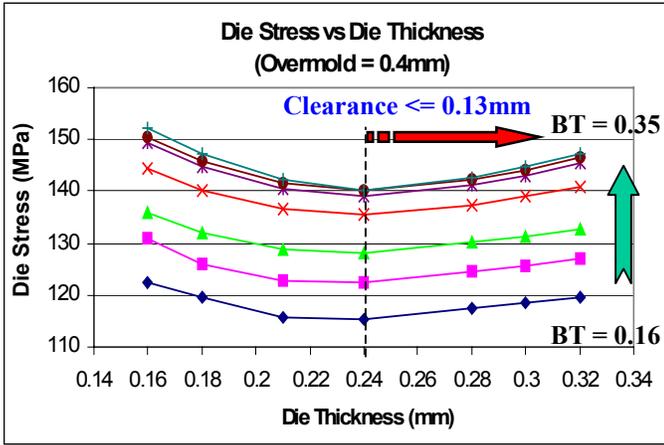


Figure 7. Trends of silicon die stress (overmold thickness of 0.4mm).

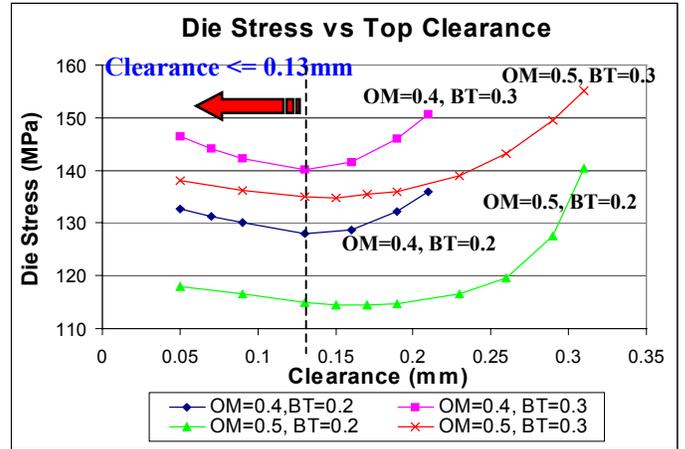


Figure 9. Trends of die stress versus top clearance.

Top and Edge Clearance Effects

Results in the earlier section highlighted the existence of a minimum top clearance for the package warpage and die stress to follow an uni-directional trend. For a more comprehensive study, die thickness for 0.5mm overmold was increased to generate FE models with top clearance of less than 0.09mm. It could be seen in Fig. 8 that the package warpage begins to decrease as the top clearance drops beyond 0.09mm. And in Fig. 9, the die stress starts to incline as top clearance falls below 0.13mm. With a very small top clearance, the FBGA package approaches a structure similar to an exposed die top. And the minimum top clearance is limited by the lowest wire bonding height (current limit of 0.18mm). Hence a top clearance of 0.13mm might not be achievable in actual case. The results showed that in the effort of obtaining low profile of the overall package height by a reduction in overmold thickness, the increase in die stress should not be overlooked.

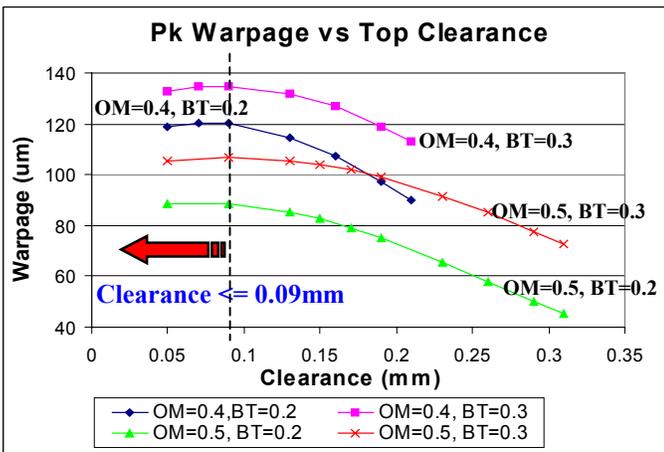


Figure 8. Trends of package warpage versus top clearance.

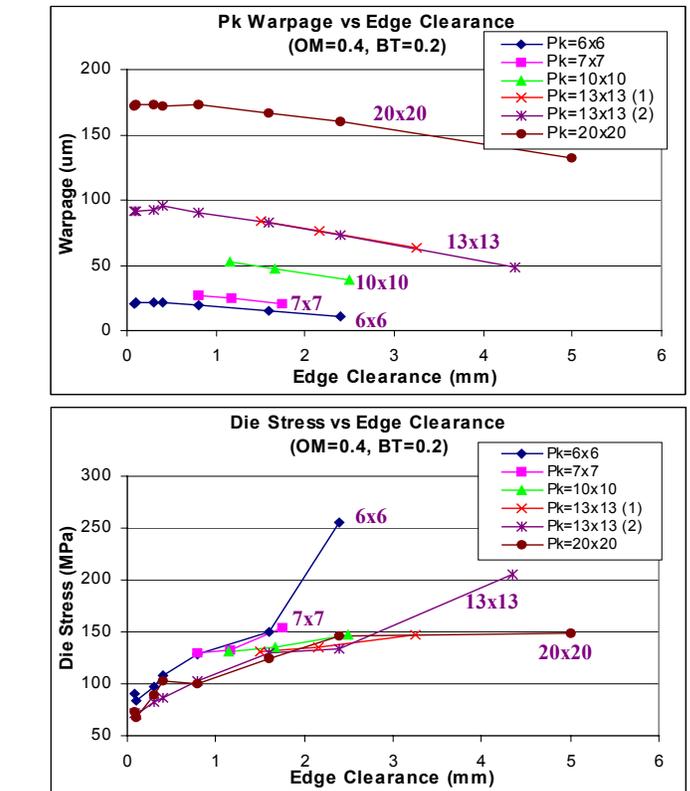


Figure 10. Package warpage and die stress versus edge clearance.

Package and Die Size Effects

The effects of package and die sizes are analyzed in this section. Commonly, the ratio for package-to-die size is made reference for design guidelines. The ratio of package-to-die (pk/die) increases as the die dimensions of a fixed package size decreases. The trend shown in Fig. 11 reflected that a lower warpage corresponded to a larger pk/die ratio. This is of similar trend observed in the effect of edge clearance (larger pk/die ratio results in a larger edge clearance). The plots of die stress revealed some important trends. In FBGA design when the package size is usually small, the ratio generally falls below the range of 2 (see Table 4). Whereas with a larger package size of PBGA, the ratio obtained are usually larger. The graph illustrated that the die stress is very sensitive to pk/die ratio when it falls within the range of 1 and 2. This implies that a FBGA package is highly subjected to die stress variation than a PBGA package. Hence careful consideration is needed for dimensional changes in FBGA packages.

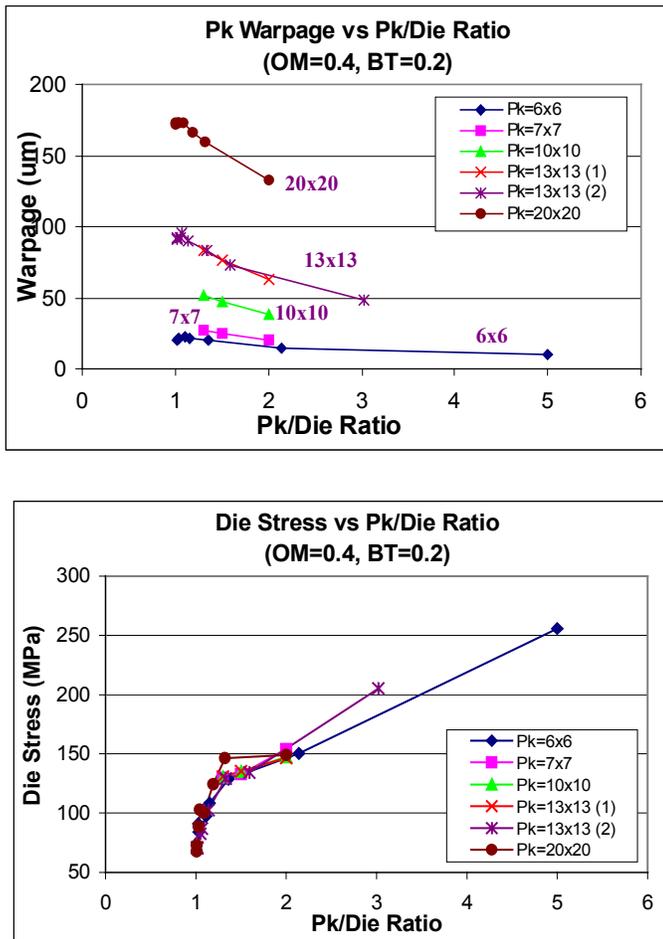


Figure 11. Package warpage and die stress versus package-to-die ratio.

Table 4. Package-to-die ratios for FBGA and PBGA packages.

Package	Pk Size (mm)	Die Size (mm)	Pk/Die Ratio
FBGA	7x7	4.6x4.6	1.52
		5x5	1.27
FBGA	13x13	10x10	1.3
FBGA	20x20	10x10	2
PBGA	35x35	6x6	5.83
		10x10	3.5

Overall Package Height Effects

With the completed study of individual effects of BT substrate, overmold and die thickness, the influence of the overall package height on warpage and die stress is being investigated. In Fig. 12, the package warpage displayed random behavior regardless of the BT substrate, overmold and silicon die thickness. As such, the warpage has shown to be independent of the overall package height. However, a decreasing trend in the die stress with the drop in overall package height is observed in Fig. 13. Earlier results showed that die stress only decreases with the decrease in BT substrate thickness, while thinner overmold and die results in stress buildup. Therefore BT substrate thickness appears to be the driving force in die stress reduction. Effectively, the use of a thinner substrate would offer a good solution in thinner FBGA productions.

CONCLUSIONS

The parametric study of a FBGA package has reflected numerous trends in the package warpage and silicon die stress. The factors that resulted in the warpage increment are thicker substrate and die, and smaller edge clearance and pk/die ratio. The decrement in die stress can be achieved by either increasing the die thickness or decreasing the substrate thickness, and having a smaller edge clearance and pk/die ratio. The trends identified have provided useful reference design guidelines for in-house designers in containing possible failures in FBGA packages.

FUTURE WORK

Further FBGA specimen can be built for warpage measurements and die crack failure correlatons. Other failure drivers such as interfaical stresses between die and mold compound could be accounted for, and the use of time and temperature dependent material properties could be implemented.

ACKNOWLEDGMENTS

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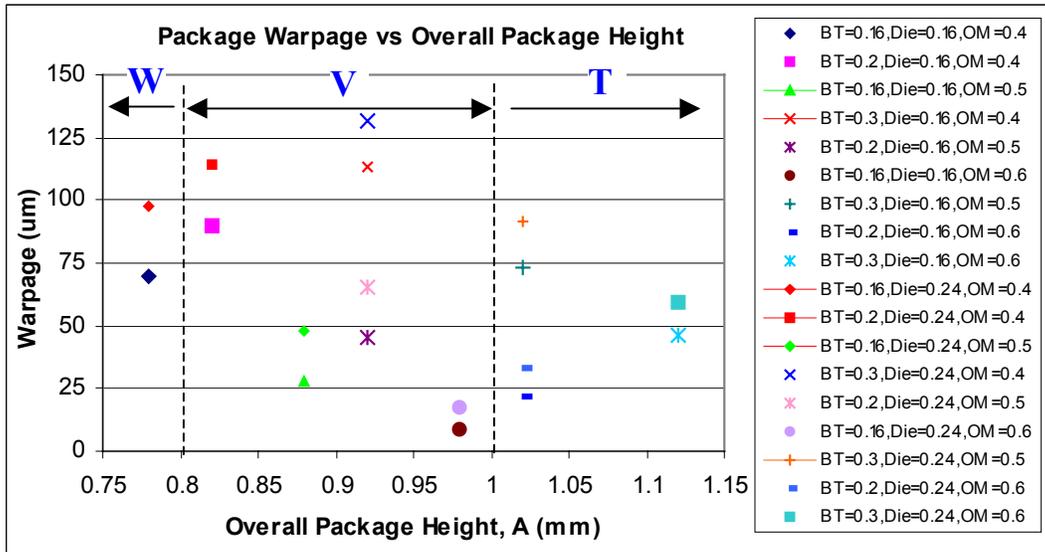


Figure 12. Trends of package warpage versus overall package height.

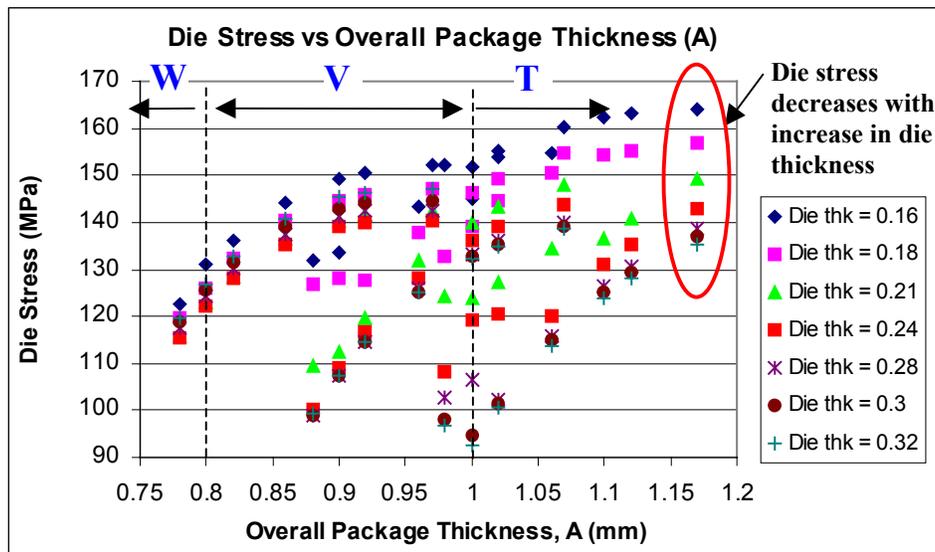


Figure 13. Trends of die stress versus overall package height.

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