Reliability Analyses for New Improved High Performance Flip Chip BGA Packages

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Abstract

High pin count and superior thermal dissipation are the main driving factors for high performance IC packages. Flip chip interconnects technology can generally achieve I/O count of more than 500, and large amount of heat in the silicon chip can be dissipated efficiently through metal heat spreader attachment. A one-piece cavity lid flip chip BGA package with high pin count and targeted reliability has recently been developed by UTAC. However it was found that solder joint reliability could be compromised due to the rigidity resulted by the one-piece cavity lid. A new design of flip chip BGA package (patent pending) has been looked into for improved board level performance. In this new design, the flip chip will be over-molded (with the die top surface exposed) before the lid is being attached. With the new single flat lid mounted onto the mold compound, the package substrate is thus less rigid under thermal loading. Hence solder joint integrity enhancement is expected. The structural differences between two flip chip BGA designs are being discussed in the paper. Test vehicles (BT substrate based) of size 40x40mm with pin count of 1521 are fabricated for the evaluation of package and board level reliability. The analysis results showed that board level reliability could be improved (of more than 50%) through design change, with no compromise in thermal performance of the package. The easy manufacturability of the flat lid has given an advantage over the complicated powder injection lid molding process, where the package cost can be reduced. Lastly, detailed package reliability of the two flip chip BGA packages is being reported.

1. Introduction

In today's era of supremacy in Information Technology and Internet communications, the demand for fast data rate transfer and high speed computing is ever increasing. This trend has inevitably presented a challenge for the electronics packaging industry in developing high performance integrated circuit (IC) packages to meet these requirements. High input/output (I/O) connections and superior thermal dissipation are the main driving focus for these packages. The advancement in flip chip interconnect technology over the years has enabled flip chip devices to be produced more cost effectively (especially on low cost BT substrates). Quality and reliability of the flip chip packages have also been improved greatly. Due its area array interconnection, much higher circuit density can be achieved comparing to conventional peripheral wire-bonding technique. To ease the significant heat generation in the flip chip device, a metal heat spreader (or lid) can be attached on the top of the package for efficient heat dissipation. In this way, the die junction temperature can be maintained at a minimum level. The heat spreader also acts as an environmental protection to the die. In addition to high thermal performance, these devices must exhibit high level of package and solder interconnects reliability, and ease in assembly process.

In conventional high performance flip chip BGA packages, a metal lid (either one-piece or two-piece structure) is directly attached onto the substrate after the flip chip assembly process. A one-piece cavity lid flip chip BGA package with high pin count and targeted reliability has recently been developed by UTAC [1]. However it was found that with the one-piece cavity lid directly mounted onto the package substrate, restricted flexing in the package has resulted in lower level of solder joints reliability when undergoing thermal cycling test. A new design of flip chip BGA package (patent pending) has been looked into for improved board level performance. In this new design, the flip chip will be plastic encapsulated (with the die top surface exposed) after the flip chip attach process. A single flat lid will then be mounted onto the mold compound (instead of the substrate). With the elimination of the direct interaction between the metal lid and substrate, the package is expected to be less rigid under thermal loading. Hence solder joint integrity enhancement is anticipated. The ease in manufacturing of the flat lid in the new design is an added advantage, as compared to the powder injection molding of the one-piece cavity lid in the original design.

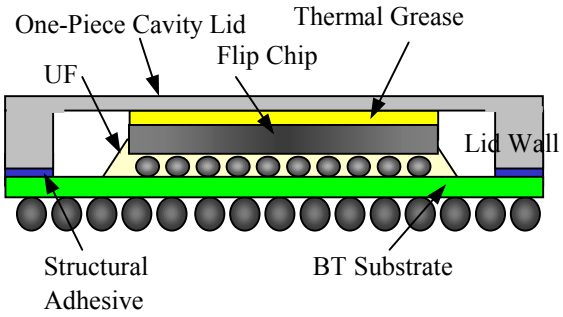
This paper discusses the structural differences between two flip-chip BGA designs. Test vehicles (BT substrate based) of size 40x40mm with pin count of 1521 are fabricated for the evaluation of package and board level reliability. With differences in the package build-up, different stress distribution within the two designs are expected. Various concerns on package reliability and warpage issue would be examined. Due to the additional molding process in the new design, the package will be subjected to post mold curing process prior to lid attachment. This process has induced extra warpage to the package, thereby increasing the difficulty in mounting the flat lid onto the flip chip surface. Ways of reducing the induced warpage such as varying mold compound properties, use of different adhesives and change in package thickness would be investigated.

In board level reliability assessment, the original design has displayed reliable performance in thermal cycling test with no solder joint failure after 1000 cycles. Finite element simulations showed that an improvement of more than 50% in fatigue life can be achieved by the new design. The observed trend would be validated with experimental data.

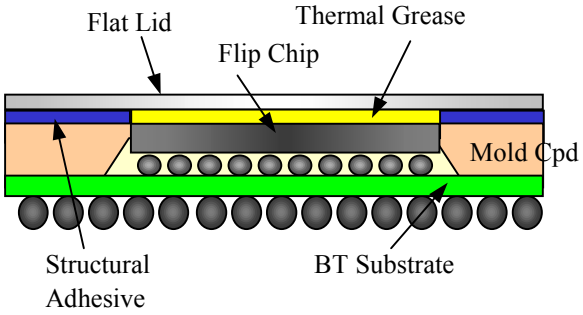
Thermal simulations were also carried out using Flotherm 3.2, with results revealing comparable thermal performance between the two designs. Experimental thermal measurement was conducted for original design according to Jedec standard JESD 51-9. With a measured θ_{JA} of 8.89 ^{o}C/W at zero windspeed, good correlation with modeling results (of 0.34% error) has been achieved. Correlation within 10% range was also obtained for forced convection conditions of 1, 2, & 3m/s windspeed.

2. Packages Construction and Configurations

A high performance flip chip BGA package (BT substrate based) of size 40x40mm as shown in Design A of Fig. 1a has been built and characterized by UTAC [1]. In design A, the one-piece heat spreader (cavity type) made of copper graphite (CuC) is mounted onto the substrate after the flip chip attach process. It was discovered that the direct interaction between the rigid lid and the substrate has restricted the flexing of the package after it was assembled onto a printed circuit board (PCB). As a result, stress and inelastic deformation of the solder joints increased with degradation in its fatigue performance. Hence a design intent is explored to reduce the direct interference between the lid and substrate.



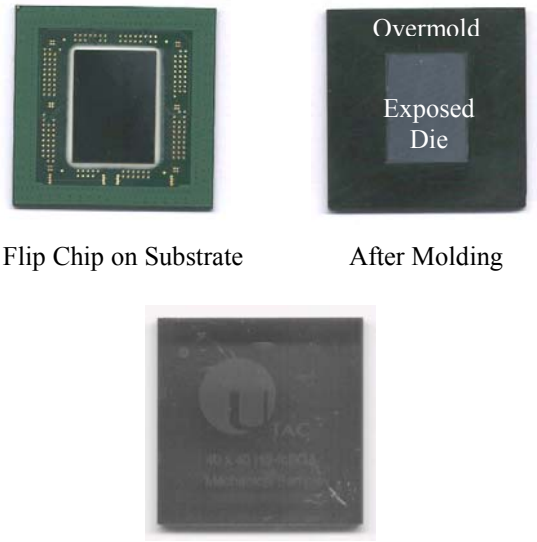
a) Design A – Original Design.



b) Design B – New Design (Patent Pending).

Fig 1. Schematic for Two Flip Chip BGA Packages.

As illustrated by Design B in Fig. 1b, the cavity type one-piece lid is being replaced by a flat lid. After the flip chip underfill process, the silicon die will be encapsulated by a layer of mold compound leaving the chip surface exposed (see Fig 2). A new mold chase was fabricated for the plastic encapsulation purpose. To provide good thermal interface with the heat spreader, thermal grease is being applied on the silicon top. And the structural adhesive is dispensed on the mold compound for adhesion with the heat spreader. The package would then be subjected to reflow at a temperature of 150^{o}C for the curing of the adhesive before solder ball mounting. With the new assembly process in Design B, the immediate interference of the lid on the substrate is thus being removed. As a result, the package is expected to be more flexible under temperature loading which eventually leads to better solder joints fatigue integrity. The actual sample of Design B is as shown in Fig. 2. In this new design, an option of low stress / high thermal conductivity structural adhesive will be evaluated. Reliability studies would be performed in comparison with the standard adhesive used.



Flip Chip on Substrate After Molding

Final Product

Fig 2. Actual Samples of Flip Chip BGA Package (New Design - B).

Both package designs share the same substrate consisting of a full array pin count of 1521 (39 x 39 rows), with a solder ball diameter of 0.6mm and a pitch of 1.0mm. The near eutectic solder composition is used in the package.

3. Reliability Testing and Conditions

The different package structure and build-up of the two designs will result in varying stress distribution and reliability performance. Package warpage in Design B after the molding process will pose a difficulty in lid attach. The finite element modeling approach will be used to study the ways of reducing package warpage and the stresses accumulated in the two packages. Assessment of the board level solder joint fatigue performance has been completed for the flip chip package - Design A. While undergoing a thermal cycling test (-40 ^{o}C to +125 ^{o}C, 1 cycle/hr), the original package design is able to survive through the industrial standard of 1000 cycles with first failure occurring at 1400+ test cycles. With the removal of the direct interaction between the lid and BT substrate, the new design is anticipated to survive longer test cycles to first failure. Finite element simulation was again employed to investigate

the impact of the mold compound encapsulation on solder joints reliability.

4. Finite Element Modeling Assessments

The finite element analysis (FEA) has been widely used in the electronic packaging industry for reliability assessment in many thermally enhanced flip chip BGA packages [2-4]. Three-dimensional (3D) FEA models were created for the two packages using *ANSYS 7.0* for stress, warpage and solder joint fatigue analysis. The 3D quarter model was created along the cut-out section A-O-B for package related study, while the 3D slice model of the section O-C was used for board interconnects analysis (see Fig. 3). The first level of flip chip interconnects (solder bumps) was assumed to exhibit the behavior of the underfill layer, hence not included in both the FE models. Inelastic strain energy density representing the damage per cycle of the solder joint would be extracted from the solution for solder joint integrity investigation.

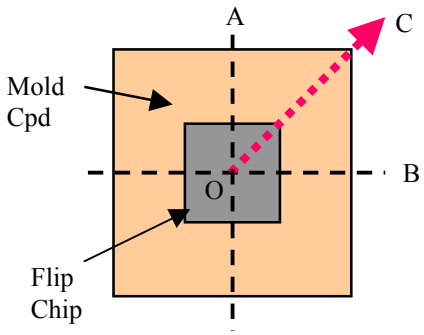


Fig 3. Package Cut-out for the 3D Quarter and 3D Slice Models.

The material properties and dimensions of the flip chip packages are listed in Table 1. Perfect adhesion is being assumed for all material interfaces. All constituent materials with the exception of the solder balls are considered to be of linear elastic behavior. Anand's model for viscoplastic material properties [5] are prescribed using ANSYS element type of VISCO107 to account for the non-linear creep behavior of the solder joints. In addition, Shi et al [6] temperature and strain rate dependent Young Modulus and yield stress are incorporated into the solder material property.

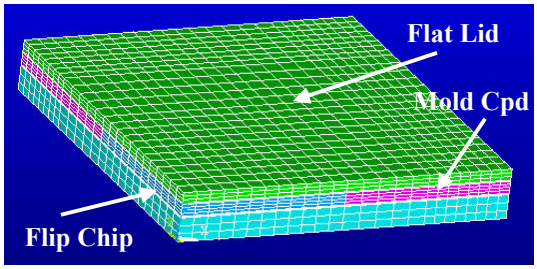
$$E = [(-0.006T + 4.72) * \log \dot{\varepsilon}] + (-0.117T + 37) \qquad (1)$$

$$\sigma_y = \begin{cases} (-0.22T + 62) * \dot{\varepsilon}^{(8.27e-5xT+0.0726)}, & for\ \dot{\varepsilon} \geq 5e^{-4}s^{-1} \\ (0.723 + 105.22) * \dot{\varepsilon}^{(1.6224e-3xT+0.1304)}, & for\ \dot{\varepsilon} < 5e^{-4}s^{-1} \end{cases} \qquad (2)$$

Table 1. Material Properties and Dimensions for the Flip Chip BGA Packages.

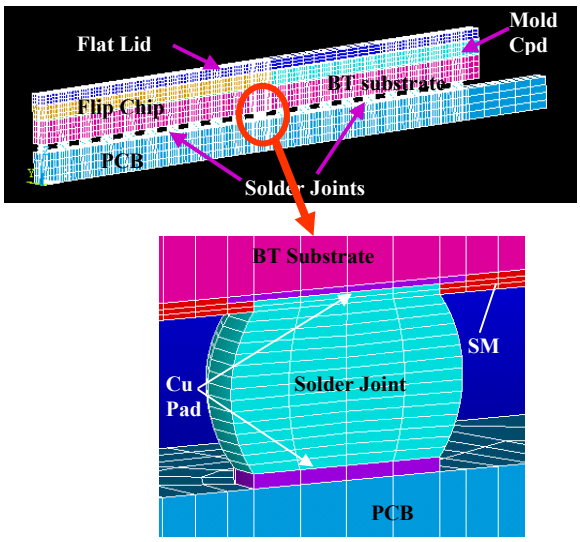
Material	E (MPa)	CTE (ppm/°C)	Poisson's Ratio	Thickness (mm)
Solder Ball	Shi's Model [6]	21	0.35	0.38 (standoff)
Cu Pad	117000	17	0.35	0.015 (Sub) 0.035 (PCB)
SM	3500	60	0.35	0.04
Die	128000	2.3	0.28	0.52
BT Substrate	25500	16 (x) 15 (y) 60 (z)	0.37	1.2 (6 layers)
Underfill	6500	$\alpha_1 = 38$ $\alpha_2 = 125$	0.3	0.08
Structural Adhesive	7000	$\alpha_1 = 48$ $\alpha_2 = 99$	0.35	0.06
Thermal Grease	0.35	232	0.35	0.06
Design A HS (CuC)	114000	15	0.35	0.51 (Top)
				0.74 (Wall)
PCB (FR4)	23000	15 (x,y) 50 (z)	0.18	1.6 (4 layers)
Design B				
HS (Cu)	127000	17.7	0.35	0.5 (Flat Lid)
Mold Cpd	27000	$\alpha_1 = 7$ $\alpha_2 = 35$	0.37	0.62
Low stress Adhesive	290	$\alpha_1 = 55$ $\alpha_2 = 135$	0.35	0.06

A thermal profile of cooling down from the reflow condition of 150°C to room temperature of 25°C was prescribed for the quarter model (Fig. 4a) at package level stress and warpage analysis. For solder joint reliability assessment, a thermal cycling loading condition from -40°C to +125°C would be applied to the slice model (Fig. 4b). Both the dwell time and ramp time equal 15 minutes. A total of three cycles of the temperature cycles would be simulated, with the stress free state at 25°C assumed. Lastly, X and Y axes boundary conditions (BC) are set to describe the symmetry planes of the flip chip packages. A third boundary condition, z = 0, is set at the bottom corner to prevent free rotation in space of the package during simulation. In addition, the "coupling" BCs are implemented on the slice model to account for constant nodal displacement on the coupled surfaces.



a) 3D Quarter Model (Section A-O-B).

Fig 4. 3D Quarter and Slice FE Models for Design B.



b) 3D Slice Model (Section O-C).

Fig 4 (cont). 3D Quarter and Slice FE Models for Design B.

5. Results and Discussion

Finite element simulations for the flip chip BGA packages were completed under different temperature loading conditions. Package level warpage and stresses, and board level solder joint reliability were assessed for the two designs.

5.1. Analysis of Package Warpage

For large package size (>20x20mm), warpage would always poses many challenges for the assembly processes. For instance, high warpage in a package will cause great difficulty in solder ball mounting onto the substrate and the eventual board assembly. With the present package size of 40x40mm for the flip chip package, it is critical to keep package warpage to a minimum. The package warpage was extracted for the finite element models after the thermal loading from 150°C to 25°C and plotted in Fig. 5. It could be seen that the original package design has generated the highest warpage, with an improvement of approximately 20% in the new design. With the use of a low stress structural adhesive, the warpage can be further improved by another 30%.

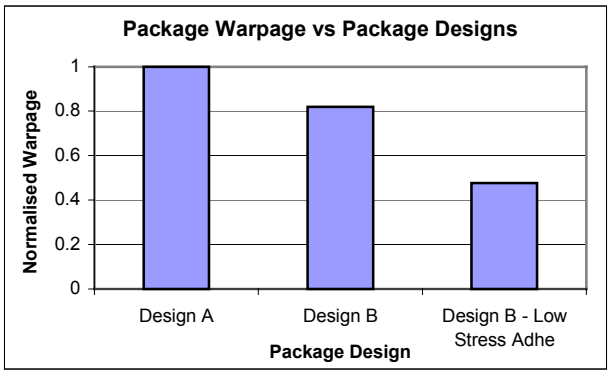


Fig 5. Package Warpage for Different Package Designs.

With the additional molding process being introduced in the new design, the package will be subjected to post mold curing before lid attachment. When the mold compound cures and set permanently, chemical shrinkage and CTE mismatch will induce further warpage to the package. In return it would increase the difficulty in mounting the flat lid onto the mold top surface. A parametric study was performed in aid of reducing package warpage (refer to plot in Fig. 6). It was discovered that an increase in substrate thickness has resulted in the decrease in warpage. The reason can be attributed to the thicker substrate that makes the package more rigid, hence less susceptable to deformation. The use of a lower Tg mold compound can also helps to reduce the package warpage. A reduction in Tg changes the effective CTE of the mold compound, giving a coupling effect on the overall CTE mismatch within the system. Lastly, the varying in die thickness and modulus of mold compound does not help much in reducing package warpage.

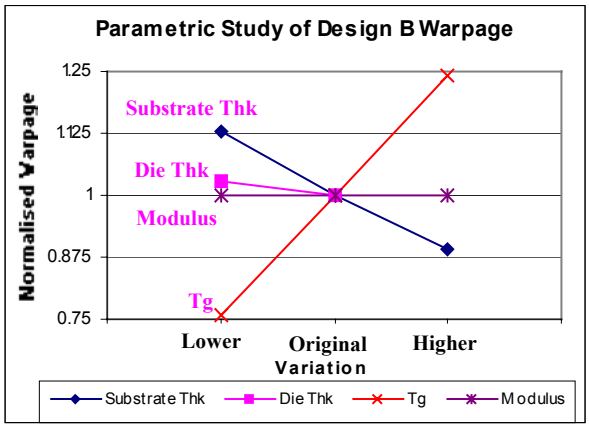


Fig 6. Parametric Effects on Design B Package Warpage.

5.2. Analysis of Package Stresses

Failures such as die cracking and interfacial delamination would render a package faulty and useless. Thus reliability of a new package under development has to be characterized effectively. The package stresses are being analyzed in this section, with focus on the flip chip and heat spreader. The silicon die being the heart and most vital part in the package, any damage to it will result in losing its electrical functionality. The heat spreader attached onto the package is able to dissipate large amount of heat away from the die and help to maintain a low junction temperature. Any failure in the heat spreader will lower its heat transfer efficiency and may result in over-heating of the silicon die. The die and heat spreader stresses, as well as their interfacial shear stresses are plotted in Fig. 7. In the die stress response, Design B generated almost 60% higher than Design A. However with the use of low stress adhesive for attaching the flat lid, comparable die stress level with Design A can be achieved. The low stress adhesive acting as an interface has reduced the interference between the lid and flip chip. Design B again reflected a higher heat spreader stress than Design A. And the low stress adhesive helps in lowering the stress level in the heat spreader. The interfacial shear stresses, where it is an indication of the adhesion strength

between interface materials, are investigated next. At the die to underfill interface, Design B with low stress adhesive has constituted to the lowest shear stress. It does indicate slimmer chances of delamination taking place at die/underfill interface compared to Design A. With attention moving to the heat spreader interface, a much lower shear stress of more than 70% decrement is being observed in Design B. With a larger adhesion area of the flat lid to the mold compound in Design B than the cavity lid to the substrate in Design A, the flat lid is able to experience a lesser shear impact. This also shows a much smaller interaction between the lid and the mold compound than the lid with the BT substrate. Thus the potential of delamination at lid interface is reduced to a minimum in Design B, enhancing the lid's capability in dissipating heat.

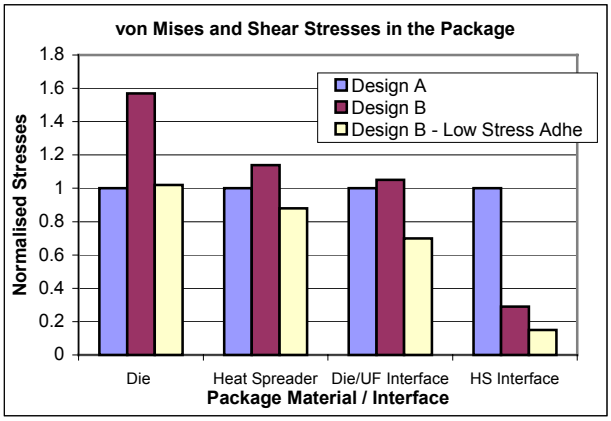


Fig 7. Stresses Experienced in Flip Chip BGA Packages.

5.3. Solder Joint Reliability Assessments

The completed thermal cycling test reliability results for test vehicles of the original design flip chip BGA package was illustrated in the Weibull plot (2 parameters) of Fig. 8. Design A reported a characteristic life, θ, of 1777 cycles (with a β of 11.3) with the first failure occurring at 1430 cycles. The widely accepted Darveaux's volume average strain energy density approach was used to calculate the solder joint fatigue lives [5]. Based on the 3D slice model simulation, a predicted fatigue life of 1214 cycles was computed. The life cycle prediction is conservative as compared to the experimental value, falling within the 1.5X correlation region. Estimated improved fatigue life was obtained for Design B package, as shown in Fig. 9. The new design showed a significant fatigue improvement of 72%. It is thus anticipated that the actual characteristic life for Design B can surpass 1777 cycles as achieved by Design A. The preceding section illustrated a significant reduction in the shear stress at the lid interface in Design B. Lesser interference is thus transmitted from the lid to the solder joints through the molding compound. The trend revealed that with the removal of the direct interaction between the lid and BT substrate, the new design is able to survive longer fatigue life cycles. This prediction is indeed very encouraging as high reliability solder joint performance is always desired for this package type and application. Test vehicles of the new design are currently in built and will be subjected to the same thermal cycling test condition. Correlation of predicted fatigue lives with experimental data would also be performed.

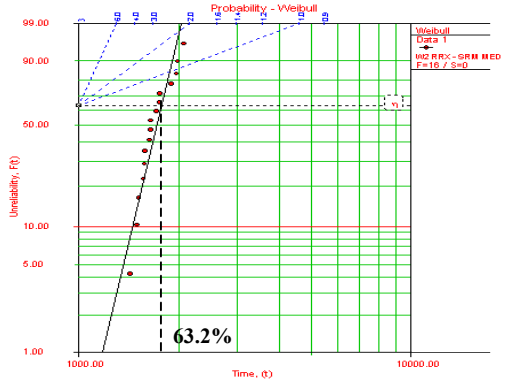


Fig 8. Weibull Reliability Data Plot for Design A Flip Chip BGA Package.

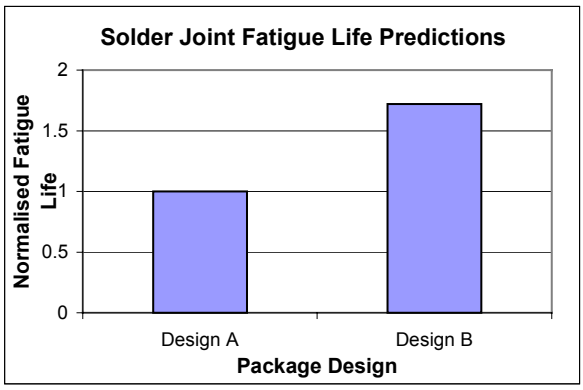


Fig 9. Solder Joint Fatigue Lives Comparison for Flip Chip BGA Packages.

In driving for higher solder joint reliability, further parametric studies have been performed on die and lid thickness. In both cases, a lower thickness has constituted to a better board level solder joints fatigue performance (Fig. 10). It is due to the lower effective CTE mismatch with the PCB by the thinner die and lid.

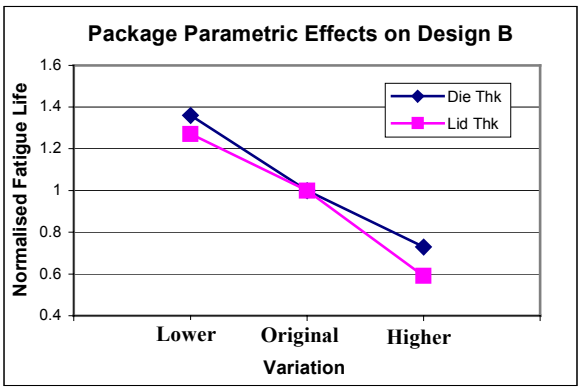


Fig 10. Package Parametric Effect on Solder Joint Reliability.

5.4. Thermal Characterization of Flip Chip Packages

High thermal performance is one of the main driving factors for the development of this package type. Hence it is necessary to ensure that the thermal performance of the new design should not be compromised. Thermal simulations were carried out using Flotherm 3.2, and experimental thermal measurement was conducted for the original design according to JESD 51-9 industrial standard. A θ_{JA} of 8.89°C/W at zero windspeed was measured, achieving good correlation with the modeling results. Correlation within 10% variation was also obtained for forced convection conditions of 1, 2, & 3m/s windspeed (see Fig. 11). Finally, thermal simulation predicted only a slight increase in θ_{JA} of 1.65% for the new design - B.

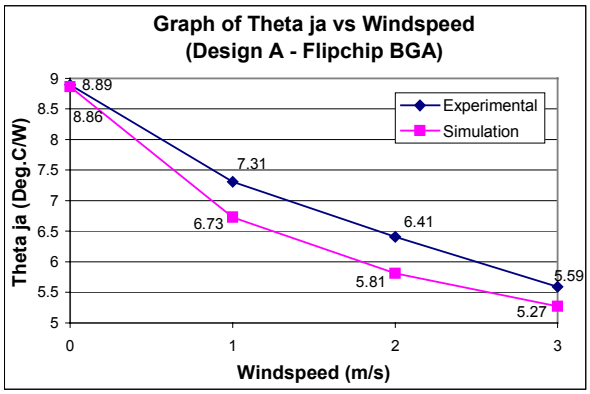


Fig 11. Thermal Measurements for Flip Chip BGA Package – Design A.

6. Conclusions

With the completed analysis based on package warpage, stresses and reliability, the new flip chip BGA package design (of either standard or low stress adhesive) is able to reveal its improved performance over the original design. In addition, there exist no compromise in thermal performance on the flip chip BGA package. The ease in manufacturing of the flat lid has also given an advantage over the complicated powder injection molding process for the cavity lid. Thus costing of the package can be reduced. Investigation also showed that the use of low stress adhesive helped in the reduction of package stresses. Parametric studies on the new design provided an indication that package warpage could be reduced by increasing the substrate thickness and the use of a lower Tg mold compound. Finally, solder joint reliability can be further enhanced by using a lower lid and die thickness.

7. Future Work

Prototype tools were used for the build of the current test vehicles of Design B. A production mode is currently under development and further reliability assessments and modeling work would be performed.

Acknowledgments

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