Heat Spreader Impact on Electrical Performances of a 4-Layer PBGA Package

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Abstract

Electrical simulations are performed for a 4-layer 388-ball PBGA package to investigate the heat spreader (HS) impact on electrical performances at high frequencies. The results show that a heat spreader, no matter floating or grounded, can help to minimize both the self and mutual inductances in a relatively low frequency range. However, a grounded HS can help to maximize the signal transmission efficiency due to low losses. In addition, grounding the HS mitigates the electromagnetic interference (EMI) issues that may occur in a floating HS case at high frequencies and at the same time helpes to push the self-resonant frequency of the package to a higher value, which effectively widens the bandwidth of the package.

1. Introduction

Lower cost, smaller form factor and many other considerations have been pushing IC chips to an ever-increasing high level integration. With more transistors integrated for insatiate high performances and multi-function purposes in a single chip, the I/O count as well as the power consumption needed are increasing. This in turn challenges the packaging of such ICs for improved electrical and thermal performances. To achieve good thermal performances, a heat spreader is usually used to help dissipate the heat generated from the chip to the ambience through the package body. However, the introduction of the HS could cause changes to the electrical performances of the system as it is usually made of electrically conductive materials. The ever-increasing processing speeds in high-speed digital systems and frequency in RF and microwave circuits makes the presence of HS much more complex in terms of its impact on system's electrical behaviors. In [1], the effect of decreasing the simultaneous switching noise of a FTBGA is demonstrated with the presence of a floating HS. Mitigation of EMI by grounding the HS is also demonstrated in [2] for a simplified BGA package by plotting the nomonized E-field at a fixed frequency point. In this paper, we investigated the HS impact on the electrical performances of a 388-ball PBGA package. Simulations are performed for the 4-layer PBGA packages for cases of without HS, with a floating HS and with a grounded HS. Using a commercially available 3D EM solver [3], S-parameters of two signal traces are extracted individually for the three cases. Based on the equivalent circuit of the package, effective inductance and resistance are extraced from the simulated S-parameters to study the HS effects on package parasitics. Frequency-dependent electric field is also computed at a radius of 3 meters away from the center of the chip to study the HS effects on Electromagnetic Interference [4,5]. In section 2, basic information of the packge will be given. Different simulation configurations are described in section 3. The simulation results are presented and dicsussed in section 4. Section 5 is the summary of this paper followed by the acknowledgement section.

2. Package Information

Shown in Fig. 1 is the cross-section of a general 2-layer HS-PBGA package.

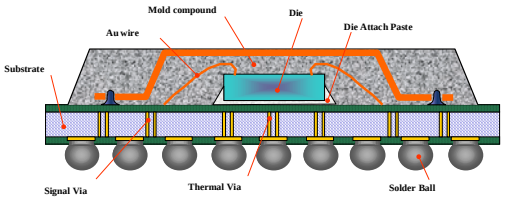


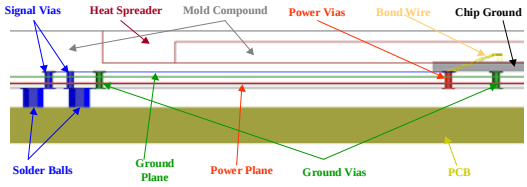
Fig. 1: Cross-section of general 2-layer HS-PBGA

For the 4-layer design, a ground and a power plane will be sandwiched in between the top and bottom signal layer, forming the stack-up of: Signal-Ground-Power-Signal with a dielectric separation distance of 100um-150um-100um. The copper thickness for the signal layer is 27um after plating and 35um for the solid ground and power plane. The package size is 35mm x 35mm x 2.35mm with a drop-in HS which has a size of 24mm x 24mm. The off-chip interconnect is achieved by wire-bonding the signal pads on the die to the top layer signal traces of the substrate, these traces are then connected by hundreds of through vias to the bottom layer signal traces where they are subsequentely connected to the solder ball arrays with a ball pitch of 1.27mm.

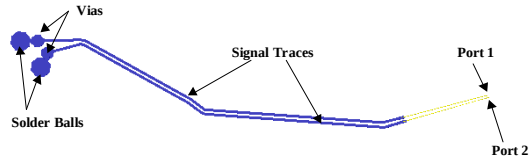
3. Simulation configurations and methodologies

3.1 Case studies

Two adjacent signal traces at one of the package corners are chosen as target nets to carry out the study. At the chip side, the power and ground plane are short-circuited to the chip ground represented by a perfect conductor through power and ground vias. At the PCB side, all the signal and power/ground balls are short-circuited to the system ground represented by a perfect-E boundary at the backside of PCB. Two lumped gap ports are assigned at the ball-end of the bond wires as the excitations. The schematics are shown in Fig. 2 for the cross-section and top view respectively.



a. Cross-section of the target nets



b. Top view with ports assigned at the bond wire ball side

Fig. 2: Cross-section a) and top view b) of target nets

The following three cases are studied:

Case 1: without heat spreader.

Case 2: with a floating 24mm x 24mm heat spreader.

Case 3: with a 24mm x 24mm heat spreader grounded to the package internal ground plane using through vias at each corner.

3.2 Modeling Methodologies

A general lumped equivalent circuit of a package with N interconnects is schemed in Fig. 3. Each interconnect is modeled with a simple RLC T-network and the couplings between them are represented by mutual inductance and capacitance.

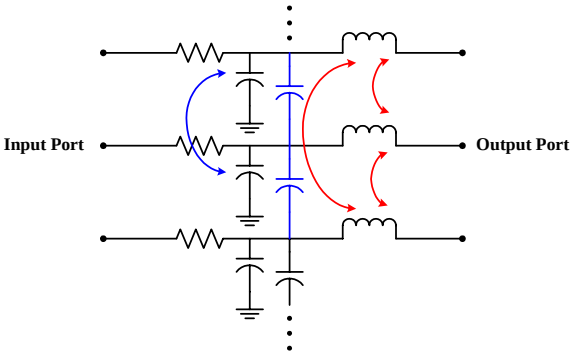


Fig. 3: General lumped model of a package with N interconnections

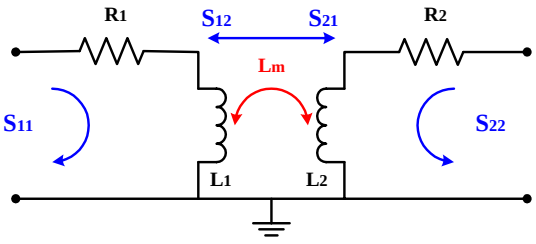


Fig. 4: Two-port RL equivalent circuit of two neighboring signal path

If short output port of all the interconnections to ground and excite them at the input ports only, the system becomes an N-port configuration and can be represented by V=Z*I. According to the definition of Z matrix, the N-port system can be separated into many two-port signal pairs to do analysis. This is because the evaluation of Z paremeters requires all the ports except the one under study to be open-circuited. Therefore, no current flows in the lumped elements. In a relatively low frequency range, the capacitance can be regarded as an open circuit element to the signal due to its high reactance. Consequently, the two-port equivalent circuit shown in Fig. 3 can be simplified into Fig. 4.

For the two-port system shown in Fig. 4, the Z parameters can be derived as:

$$Z_{11} \approx R_1 + j\omega L_1 \quad (1)$$

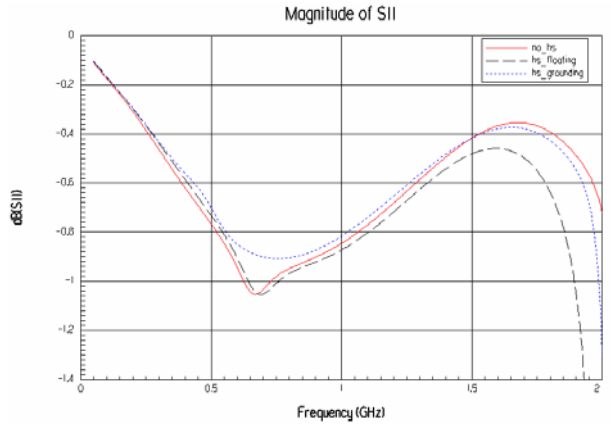
$$Z_{22} \approx R_2 + j\omega L_2 \quad (2)$$

$$Z_{21} \approx Z_{12} \approx j\omega L_m \quad (3)$$

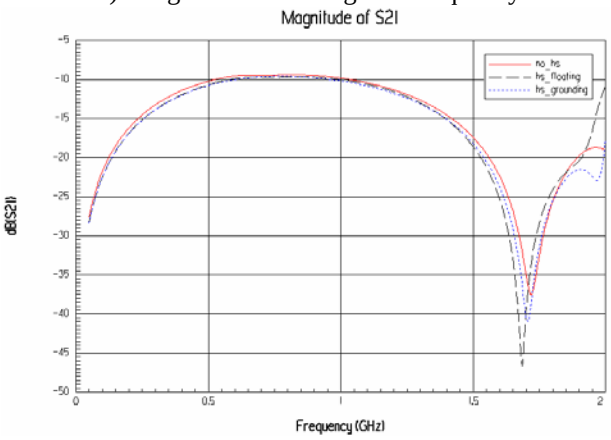
Thus, the resistance and self/mutual inductance can be derived from the real part and imaginary part of the Z parameters, respectively. The above-mentioned method is well documented in [6] and was widely used as a method to do package characterization for modeling, simulation and measurement.

4. Results and Discussions

The simulations are performed for the three cases in the frequency range of 0.05-2GHz. Magnitude of S11 and S21 are plotted in the cartesian coordinate system in Fig. 5 to show the energy transmission through one net and isolation between the two nets.



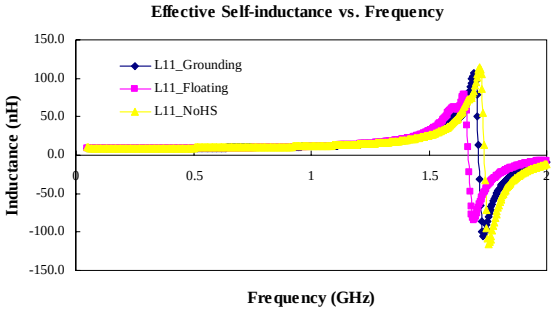
a). Magnitude of S11 against frequency



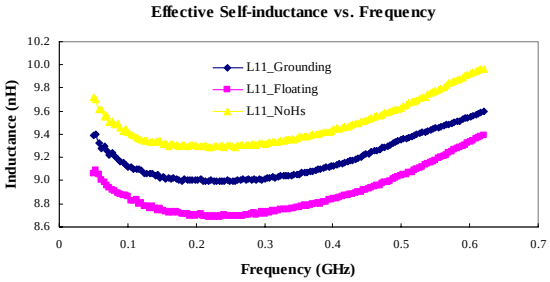
b). Magnitude of S21 against frequency

Fig. 5: Magnitude of S11(a) and S21(b) vs. frequency

From Fig. 5, we can see that case 3 has the highest signal transmission efficiency and the presence of a heat spreader can help to improve the isolation between the two signal nets which is in fact an improvement of crosstalk.

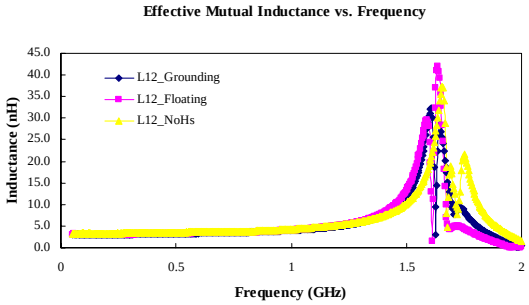


a). Effective self inductance in a frequency range of 0.05-2GHz

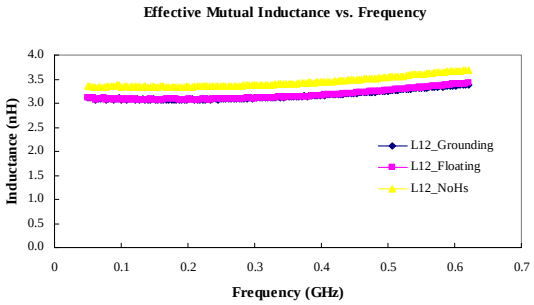


b). Effective self inductance in a low frequency range

Fig. 6: Effective self inductance of one of the two target nets

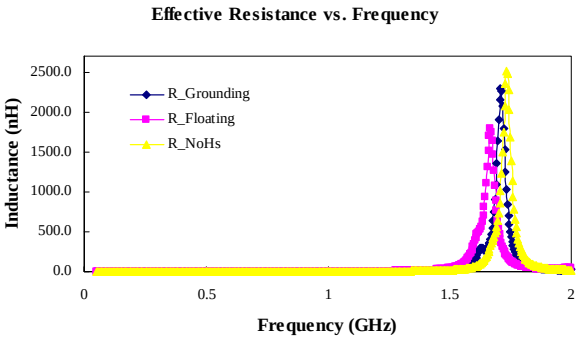


a). Effective mutual inductance in a frequency range of 0.05-2GHz

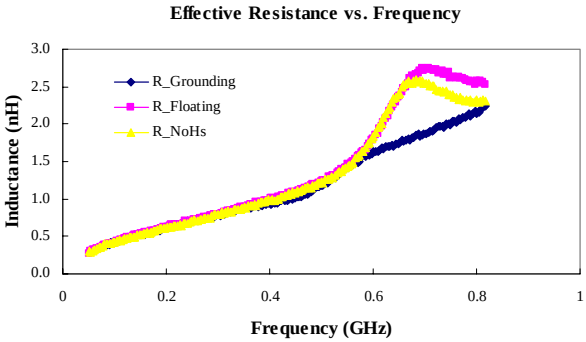


b). Effective mutual inductance in a low frequency range.

Fig. 7: Effective mutual inductance of one of the two target nets



a). Effective resistance in a frequency range of 0.05-2GHz



b). Effective resistance in a low frequency range.

Fig.8: Effective resistance of one of the two target nets

To investigate the impacts on package parasitics caused by different HS configurations, the effective resistance and self inductance of one net and the mutual inductance between the two nets are extracted using the method discussed in section 3.2 and plotted in Fig. 6-8.

Fig. 6 through Fig. 8 show that case 1 has the highest self and mutual effective inductance among the three cases. A heat spreader, no matter floating or grounded, can help to minimize both the self and mutual inductances in low frequency range. Although, a floating HS is most efficient in reducing effective inducances, the grounded HS can maximize signal transmission due to the relatively low losses as was shown in Fig. 5 and Fig. 8, respectively. Effective inductance and resistance value peak up when resonance occurs, it is clearly shown in Fig. 6 and Fig. 8 that grounding the HS can help to push the self-resonant frequency of the package to a higher value, which effectively widens the bandwidth of the package.

Shown in Fig. 9 is the plot of computed E-field at 3 meters from the chip center. The obervation point of the E-field is right above the package in the Z direction assuming that the package is located in the XY plane. The surface current plots on the HS are depicted in Fig. 10 for case 2 and case 3 respectively, at 1.67GHz what is approximately the resonance frequency of the package.

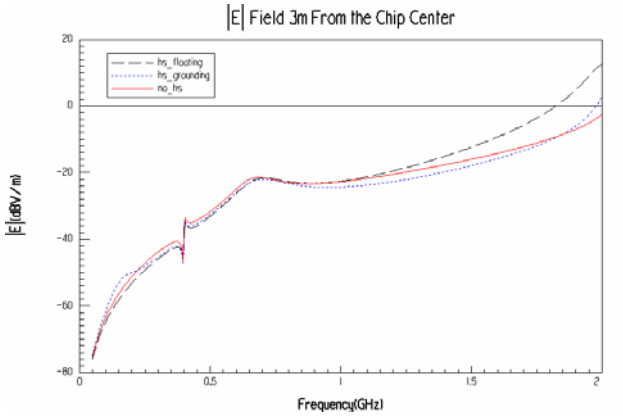
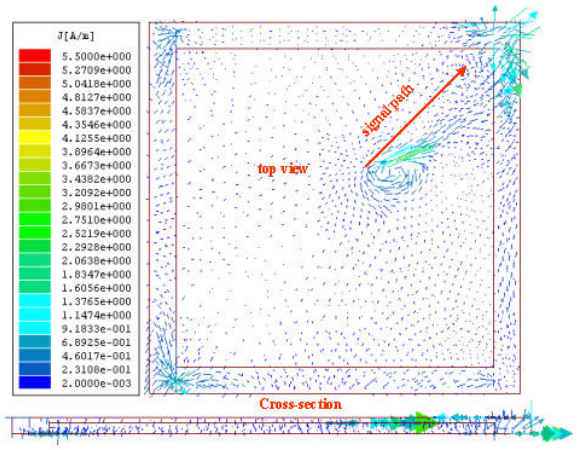
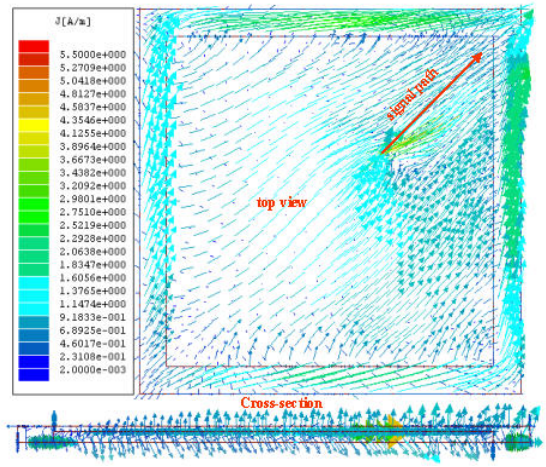


Fig. 9: E-field 3m from the chip center against frequency



a). Grounding HS



b). Floating HS

Fig. 10: Surface current plot of a).grounding and b).floating HS case

Fig. 9 indicates that a floating HS has a shielding effect on the package, resulting in an improved EMI at low frequency range. However, it couples the energy from the chip at high frequencies and begins to act as a radiator. This radiator effect can be mitigated by grounding the HS internally to the package ground reference plane. Strong radiation is observed when the signal trace resonance occurs at a frequency point a little beyond 1.5GHz. The power-ground plane cavity resonance phenomenon is also captured cleary on the E-f plot at around 400MHz. It is obvious that the radiation caused by the cavity resonance at low frequency range is insignificant compared with the radiation caused by the signal trace resoance at a much higher frequency range. The surface current plot of HS shows very clearly the proximity and current crowding effect. As can be seen from Fig. 10b, there is no current return path for the crowding current on the surface of the floating HS to escape, it results in a larger effective resistance and stronger free-space radiation, causing higher energy losses and more severe EMI issues.

5. Conclusions

As a summary, simulation of a 388-ball 4-layer PBGA package indicates that a floating HS can reduce the parasitic self and mutual inductances of the signal traces. This will result in a smaller SSN and crosstalk respectively, without causing EMI issues in a low frequency range. By grounding the heat spreader to the package ground reference plane, a maximum power transmission, wider device bandwidth and minimized high frequency radiation can be achieved.

6. Acknowledgments

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