Reliability assessment for Cu/Low-k structure based on bump shear modeling and simulation method

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Abstract

Bump shear is widely used to characterize interface strength of Cu/low-k structure. In this work, the blanket low-k structure was used to evaluate the reliability and strength of Cu/low-k structure using finite element modeling technique. The objectives of this work are to determine the critical stress parameters for low-k interfaces with different Cu/low-k structures for understanding the failure mechanism and to improve the low-k structure reliability by optimizing the some parameters. In this paper, the comprehensive parametric study was conducted including 3 different low-k structures, different shear ram height, high Pb solder vs. Pb-free solder, different UBM thicknesses, blok layer modulus effect. The simulation findings can be summarized as follows: The shear force decreases with shear ram height. The critical stress decreases with the number of layer of low-k structure. Higher shear force occurs for SnAg solder bump than SnPb one. Reducing UBM thickness can help to improve the low-k structure reliability.

1. Introduction

With the increasing requirement in speed of advanced integrated circuits, the copper/low-k structures are the desired choice for replacing traditional aluminum/SiO_2 structure in chip interconnection due to some benefits for Cu/low-k structure such as reduced interconnection RC delay, less crosstalk and lower power loss. However, the reliability of Cu/low-k structure becomes the great concerns due to poor interfacial adhesion and lower modules for low-k material. Therefore, the effects of flip chip packaging or wire bonding process on reliability of Cu/low-k structure become the critical concerns because stress induced in these processes can result in Cu/low-k structure failure [1-3].

The mainly failure mode for Cu/low-k package is the interface brittle cracking failure between low-k material and metal layer during wire bonding or solder bumping process due to weak interface strength [4,5]. Bump shear is widely used to characterize interface strength of Cu/low-k structure. The objectives of this work are to determine the critical stress parameters using finite element modeling method for low-k interfaces with different Cu/low-k structures for understanding the failure mechanism and to improve the low-k structure reliability by optimizing the some parameters. In this paper, the comprehensive parametric study was conducted including 3 different low-k structures, different shear ram height, high Pb solder vs. Pb-free solder, different UBM thicknesses, blok layer modulus effect. The simulation findings can help to improve the low-k structure reliability when subjected to mechanical loading.

2. Low-k Structure and FE Model

In this study, the blanket low-k structure was used to assess the strength of low-k/metal interface. The sample is show in Fig. 1. Three low-k structures as shown in Fig. 2, such as 1-layer, 15-layer and 18-layer, were evaluated using finite element method to investigate the number of low-k structure layer effect on interface strength. The bump shear test was conducted for low-k structure. The failure of interface delamination between low-k (BD layer) and blok layer (SiC) was found by TEM as shown in Fig. 3. From Fig. 3, the fist low-k layer/blok interface under the bump is prone to delamination failure then other interfaces. Usually the BD lok-w layer has lower Young's modulus and adjacent layer has higher modulus, thus reduces the interface strength between low-k and adjacent layer due to modulus mismatch and brittle features of low-k layer.

The bump shear FE simulation and parametric study were carried out to assess the low-k structure reliability and explain the failure mechanism. In this work, some parameters, such as shear ram height, different blanket low-k layers, bump material of high Pb vs. Pb-free solder, UBM layer thickness and blok layer material properties, were considered in FE simulation to investigate their effect on stress-strain behavior of blanket low-k structure.

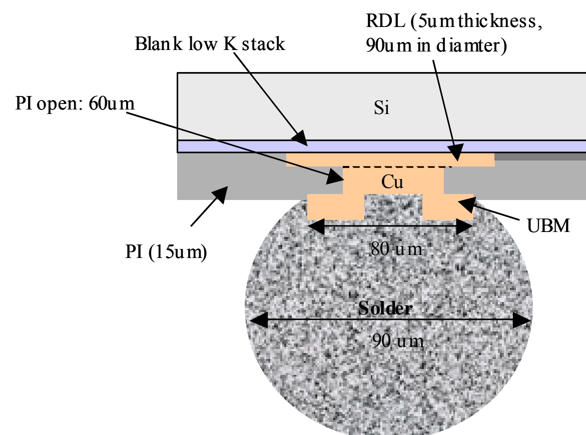

Fig. 1. Solder bump sample with blanket low-k structure

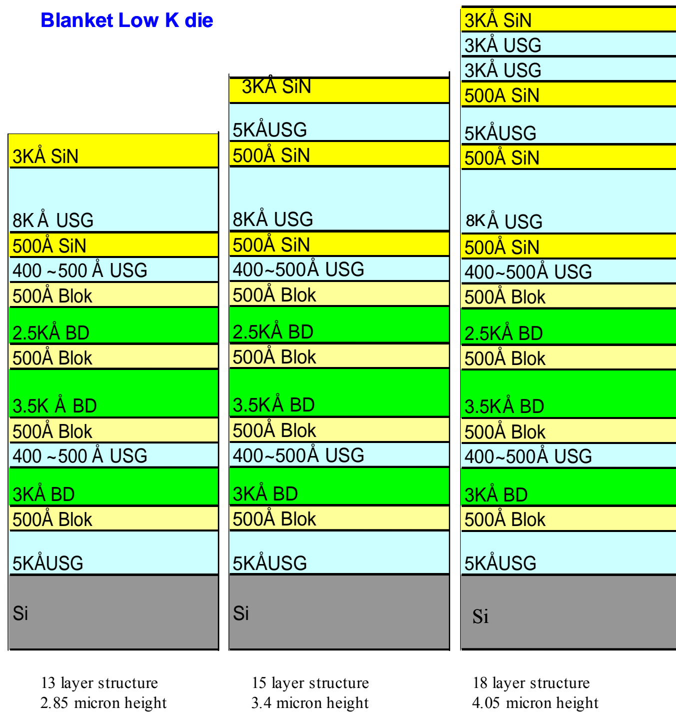

Fig. 2. Three blanket low-k structures

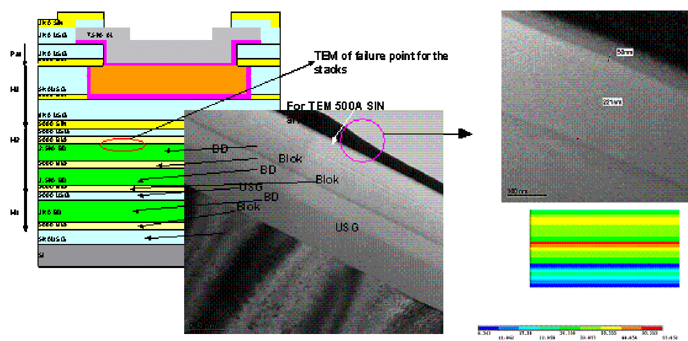

Fig. 3. TEM image showing blok/low-k interface failure

In this work, 2D plain strain FE model as shown in Fig. 4 was used to assess the reliability of low-k structure under the bump shearing force. The die thickness of 100µm was implemented in the FE model. The die width was selected as twice of solder bump diameter to reduce the boundary effect on stress-strain distribution of low-k structure under the bump. All nodes of die bottom side were fixed in all direction to avoid the rigid body movement. The shear speed was 100µm/s. Table 1 listed the material properties used in FE simulation. The UBM layer material was modeled as bilinear plastic behavior. The solder bump material was modeled as elastic-plastic with perfect plastic behavior. The other materials were just considered as elastic behavior. The shear ram was modeled as rigid part without deformation. The face-to-face contact between shear ram and solder bump surface and contact between solder bump surface and PI layer were created in FE model. Three FE models with different low-k structure layers of 1-layer, 15-layer and 18-layer were simulated to investigate the number of layer effect on stress-strain distribution, respectively. The parametric study including shear ram height effect, solder bump material effect, UBM thickness and blok layer material properties effect on reliability of low-k structure, were performed based on FE model with 13-layer low-k structure. The detailed simulation result analyses were described in the sections below.

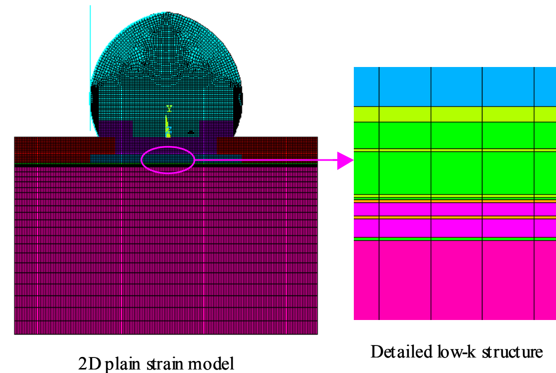

Fig. 4. 2D FE model for bump shear simulation

Table 1. Material properties used in FE model.

Materials	CTE (ppm/°C)	E (GPa)	Poisson ratio	Density (kg/m3)
Silicon Die	2.7	131	0.28	2330
Low-k (BD)	23	7.7	0.3	1500
USG	0.57	66	0.18	2330
RDL	17	110	0.34	8920
Dielectrical (PI)	57	4.0	0.35	1310
Cu pad & UBM	17	E = 130.0; σy = 137.9MPa Tangent modulus 0.365	0.34	8960
5%Sn/95%Pb	29	E=23.5; σy = 13.3MPa	0.35	11130
Sn / 2.5% Ag	21.7	E=51; σy = 22.5MPa	0.3	7360
SiN	2	210	0.27	3190
Blok (SiC)	3.8	420	0.3	3170

3. FE Simulation Result Discussion

Shear ram height effect: The gap between shear ram and die surface was defined as shear ram height as shown in Fig. 5. In this model, the solder bump height of 75µm and UBM thickness of 10µm were modeled. The SnAg lead free solder bump was considered. The shear ram heights of 5% (3.75µm), 10% (7.5µm), 15% (11.25µm) and 18.3% (13.75µm) of bump height were simulated, respectively.

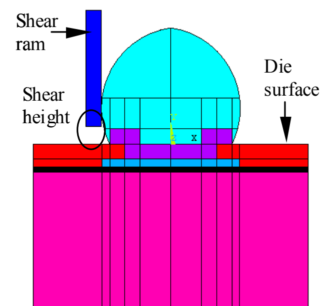

Fig. 5. Definition of shear ram height

Fig. 6 shows the shear ram height effect on shear force. It can be seen that shear ram height affects on shear force significantly, and shear force decrease with ram height. For shear ram height with 5% and 10% of bump height cases, it is difficult to obtain the converged shear force because shear ram height is less than UBM thickness. When shear ram height (11.25μm and 13.75μm) is more than UBM height (10μm), the converged shear force can be obtained and shear force value is similar when the shear displacement is more than 3μm. Modeling 5μm shear displacement is enough to obtain converged shear force because almost all solder elements with closing to solder/UBM interface yield, which can be seen from Fig. 7. In the following modeling and simulation, the shear ram height with 15% of bump height will be implemented.

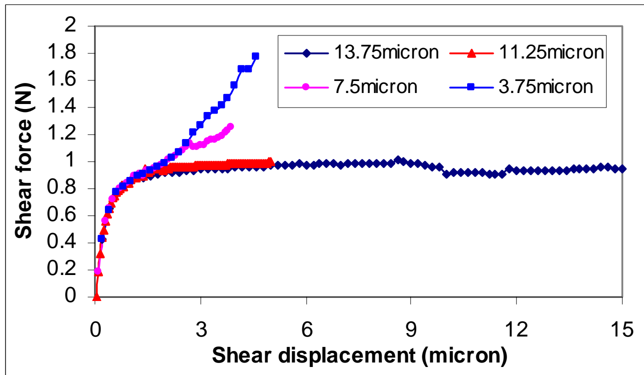

Fig. 6. Relationship of shear force and shear displacement for different shear ram height cases

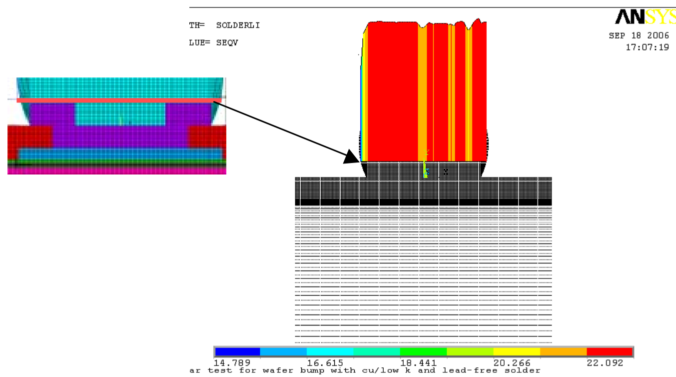

Fig. 7. von Mises stress contour along solder/UBM interface

Bump material effect: In this work, the lead free solder bump of 97.5%Sn2.5%Ag and high Pb solder bump of 5%Sn95%Pb were simulated to study their effect on shear force and stress-strain behavior of low-k structure. Fig. 8 shows the relationship between shear force and shear displacement. It can be seen that the converged shear force is higher for SnAg solder bump case compared to the high Pb solder bump case due to higher yield stress value for SnAg solder material. The linear relationship between converged shear force and solder yield stress can be obtained from equations (1) and (2).

$$\text{Shear force}_{SnAg} / \text{Shear force}_{high\ Pb} = 0.994/0.588 = 1.69 \quad (1)$$

$$\text{Yield stress}_{SnAg} / \text{Yield stress}_{high\ Pb} = 22.5/13.3 = 1.69 \quad (2)$$

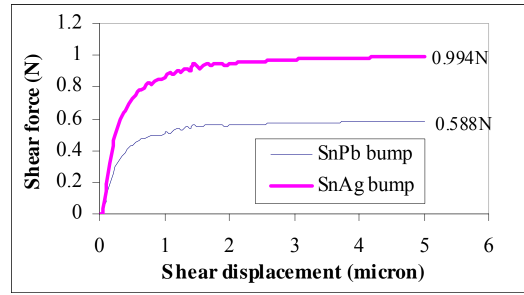

Fig. 8. Solder bump material effect on shear force

The higher shear force will induce higher stress level in interface layers of low-k structure. Usually, the peel stress is one dominant parameter to induce the interface delamination. The peel stress contour as shown in Fig. 9 shows that the critical area of blank low-k die is under the shear ram, which is the area prone to cracking or delamination due to large peel stress. The maximum peel stress occurs on the top interface of blok/BD low-k layer as shown in Fig. 9, which is consistent with the delamination location from TEM analysis as shown in Fig. 3. The adhesion strength of interface between blok and BD low-k layers is usually weak, so the delamination failure along this interface is one important failure mode for Cu/low-k die structure under mechanical or thermomechanical loading.

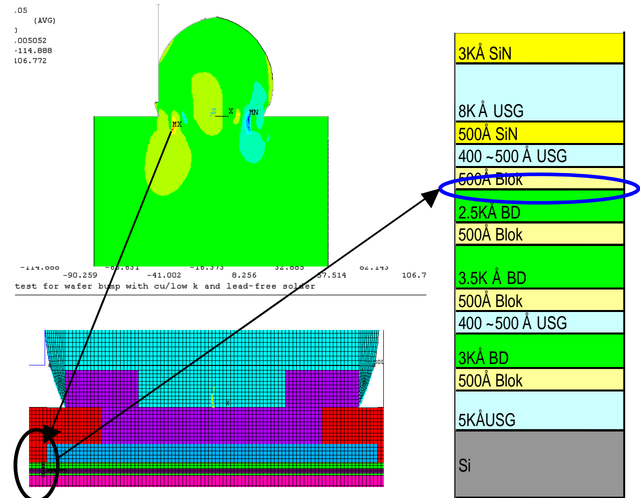

Fig. 9. Critical peel stress location from FE simulation

Fig. 10 shows the stress distribution along BD/blok interface. The left half part of interface close to shear ram shows the peel stress, while the right half part of interface far away from shear ram shows the compression stress. It also can be seen from Fig. 10 that the maximum peel stress is higher when using SnAg as solder bump material than using high Pb as solder bump material. Therefore, solder material effect on reliability of low-k structure is significant. Usually, high Pb or eutectic SnPb solder has lower elastic modulus and is softer than SnAg lead free solder. The Cu/low-k structure interface delamination failure is prone to happen when using SnAg solder as bump material.

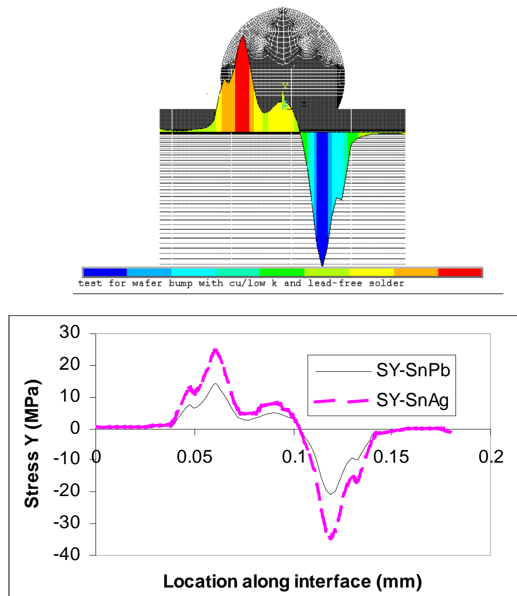

Fig. 10. Normal stress along the critical BD/blok interface

The number of low-k structure layer effect: Three blank low-k structures with 13-layer, 15-layer and 18-layer as shown in Fig. 2 were simulated in this work to investigate the different structure effect on interface stress and reliability. From simulation result, the top BD/blok interface layer adjacent to the solder bump is critical stress location for all low-k structures. The maximum peel stress and shear stress along top BD/blok interface were listed in Table 2 for different structures. It can be seen that both maximum peel and shear stresses decrease with the number of layer of low-k structure for both SnAg and high Pb bump cases. It can be seen from Fig. 2 that the distance from top BD/blok interface to shear ram increases when more layers are used in low-k die, which will reduce the stress level transferred from solder bump to BD/blok interface.

Table 2. Comparison of maximum stress along BD/blok interface for different structures

Solder bump	Layers	Sy (MPa)	Sxy (MPa)
high Pb	13layer	14.3	7.46
	15layer	13.8	7.17
	18layer	13.2	7.15
SnAg	13layer	24.6	12.68
	15layer	23.8	12.2
	18layer	22.8	12.18

The elastic modulus of blok layer effect: The BD low-k layer shows the brittle behavior and has lower elastic modulus. The adjacent blok layer has higher elastic modulus and higher hardness, so the modulus and hardness mismatch between BD low-k and blok layers will induce their interface weak. In this study, the elastic modulus of blok layer material effect on interface stress was investigated. The elastic moduli of 420GPa, 70GPa, 35GPa 15GPa, and 5GPa were simulated for blok layer material, respectively. Fig. 11 shows the elastic modulus effect on maximum stress of BD/blok interface layer. It can be seen that both maximum peel and shear stresses increase with elastic modulus of blok layer slightly. This result provides the guideline for material selection to reduce the interface stress when solder bump subjected to mechanical loading.

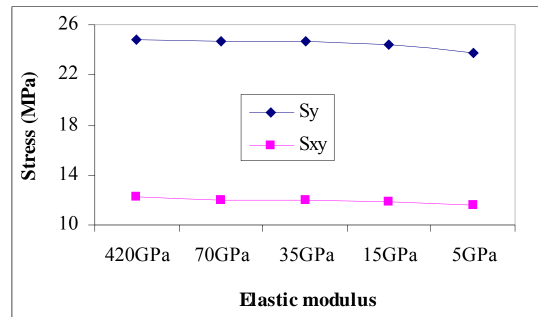

Fig. 11. Elastic modulus effect on interface maximum stress

UBM thickness effect: The UBM thickness of 10μm was molded in all the above simulations. Another UMB thickness of 2μm as shown in Fig. 12 was also simulated to investigate the UBM thickness effect on shear force and interface stress. It can be seen from Fig. 13 that shear force increases with UBM thickness. Fig. 14 shows the UBM thickness effect on stress distribution of BD/blok interface when shear force is stable. It can be seen that thicker UBM induces the higher peel stress, which results in the interface delamination failure more easily. Fig. 15 shows the UBM thickness effect on maximum peel and shear stresses of interface layer. It can be seen that the both peel and shear stresses increase with UBM thickness and the UBM thickness effect on peel stress is more significant than shear stress.

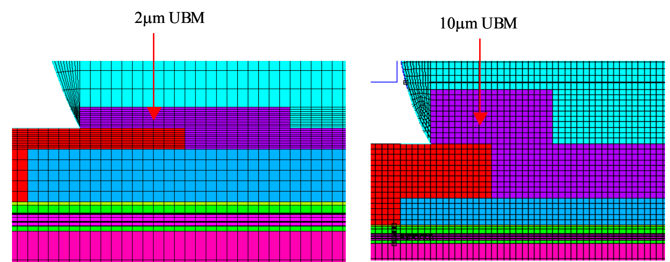

Fig. 12. Partial FE models with different UBM thickness

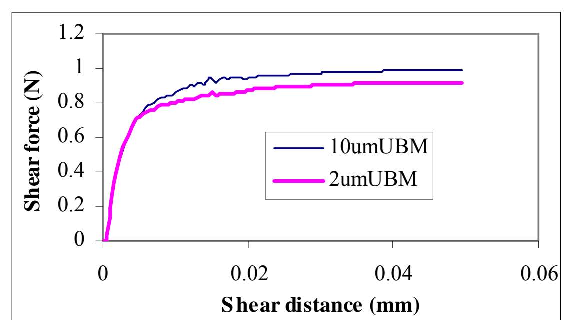

Fig. 13. UBM thickness effect on shear force

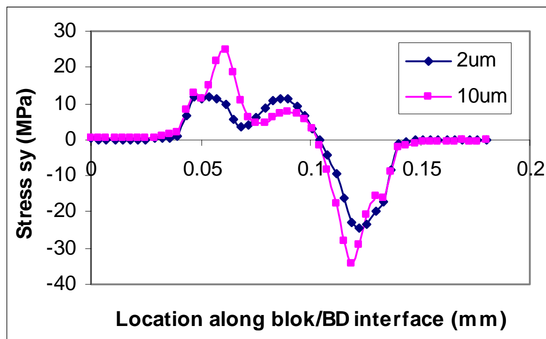

Fig. 14. UBM thickness effect on stress distribution along blok/BD interface

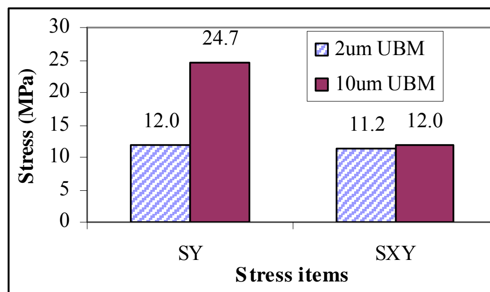

Fig. 15. UBM thickness effect on maximum stress of blok/BD interface

Conclusions

The reliability assessment of blanket low-k die structure was developed based on bump shear modeling and simulation with comprehensive parametric study. The critical failure site of top blok/BD interface layer was achieved from simulation and testing result. The findings from bump shear simulation can be summarized as blow:

1. Ram height has significant effect on shear force and shear force decreases with shear ram height. When the ram height is more than UBM height, the similar converged shear force can be obtained after 5μm shear displacement.

2. Solder material effect on shear force and interface stress value is significant, the SnAg bump results in the dangerous condition in terms of interface peel stress compared to high Pb bump case.

3. Different low-K die structures lead to almost same shear force. However, more low-k structure layers reduce the stress of blok/BD interface layer.

4. Blok/BD interface stresses increase with elastic modulus of blok layer material, selecting blok material with lower modulus can improve the low-k structure reliability.

5. Thinner UBM thickness results in lower shear force and interface stresses.

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