Copper Clip Package for high performance MOSFETs and its optimization

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Abstract

Copper clip package plays a critical role in meeting the increasing requirement for lower total device resistance RDS(on), higher power density and high frequency switching applications. The copper clips replaced traditional wirebond interconnect for high performance MOSFETs by providing lower resistance and inductance than multiple wirebonds and improves thermal performance. This paper will discuss about the research and development efforts from different stages of package's development from simulation, analysis and process optimization of array clips assembly of this package.

Comprehensive mechanical, thermal and electrical analyses are performed for a power module with stringent requirement. Thermal simulations are performed to study the impact of attachment voids and the thermal advantages of copper clip. Electrical simulation shows the comparison of copper clip over multiple copper wires. Design for process optimization such as array bonding, high speed bond head and high performance clip singulation system are discussed as well.

Key learning from this study can be used to formulate database and guidelines for upfront product enhancement, reduce the design-to-implementation cycle time, identify high risk before fabrication and troubleshooting during production. Collaborative approach with simulation can save time and resources, hence increasing efficiency and reducing cost as well as development cycle time.

Introduction

Quad Flat No lead (QFN) packaging is broadly accepted by the semiconductor industry owing to low cost, small footprint, good heat dissipation with ability to implement die attach paddle (DAP) underneath the Die and lower electrical parasitic parameter. Low on-state resistance (RDS(on)) is the key characteristic for a power device and it is contributed by silicon Die and package's interconnect parasitic. However, silicon resistance is greatly reduced by new development in MOSFETs technology and package's resistance becomes a major concern to achieve lower RDS(on). [1] QFN package is widely used in the industry for power MOSFETs to make use of DAP as a Drain pin and multiple heavy wires (thick copper or aluminum wire bonding) to address high resistance between Die top and leadframe. Since the Die with back side metal is directly attached to the copper block (DAP), its' resistance is less significant compared to Die top interconnect whereas reduction in resistance is limited by cross sectional area of the wires. Ribbons with larger cross sectional area than heavy wires will further reduce Die top interconnect resistance. However, Copper Clip enables direct soldering on Die's top surface to utilize full Die's top metallization. This allows largest possible contact area and lowest resistance than ribbons and wires. Electrical performance comparison between Cu Clip and thick wires will present in this paper.

Copper Clip QFN packages are targeting for power management products ranging from telecommunication, computing and battery management. Efficient power management is crucial for increasing demands on high definition mobile video streaming, 4G network communication and longer battery life, etc. UTAC developed Copper Clip QFN package for high performance MOSFETs, replacing multiple Copper or Aluminum wires with lower electrical impedance (low RDS(on)), better thermal performance and high reliability. Figure 1 shows discrete clip option and multiple clips bonding with stacked clips options.

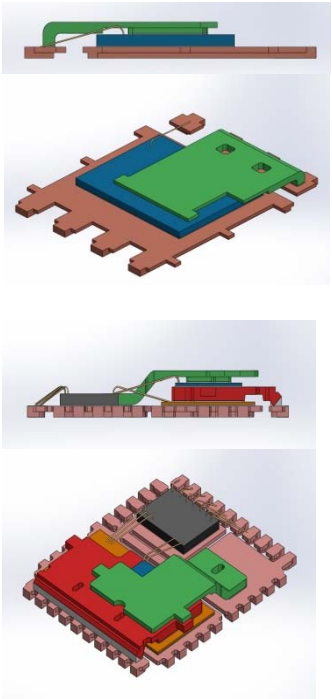


Fig. 1. Power packages with discrete clip and stacked clips

Cu-clip QFN assembly process flow is shown in Figure 2 and clip configuration is available with directly soldered on Die's top metallization. The assembly process starts with front of line (FOL) process where die attach, clip attach and wire bond are performed.

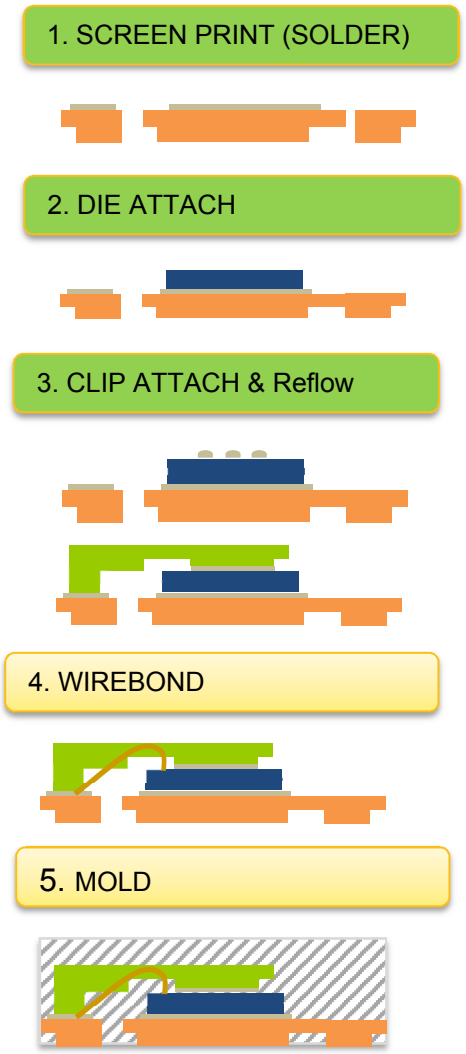


Fig. 2. Cu-clip QFN packaging process flow

During FOL process, key processes are performed; solder print or dispense, Die and Clip attach and solder reflow. As illustrated in Figure 2, screen-print technology is used to deposit the solder on DAP for MOSFET Die attach and on lead for Clip base attach. Then followed by Die attached, solder dispense on Die, clip attach and solder reflow.

Fig. 3. High speed bond head system

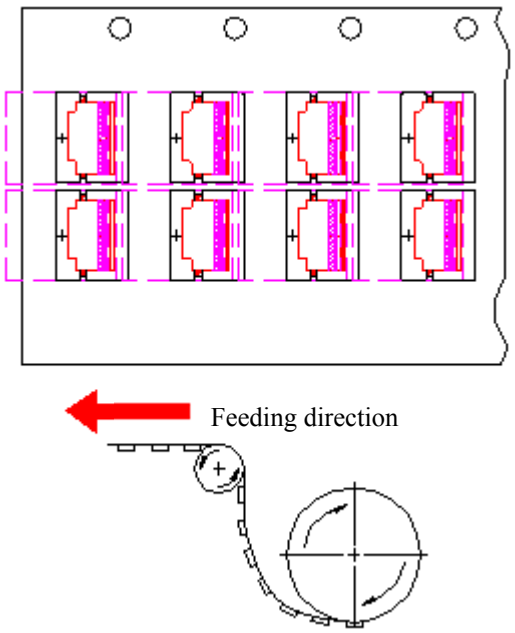


Fig. 4. : Cu-clip in reel form

The Clip bonder is capable of array bonding up to 20 clips at the same time. Array bonding enables for faster process cycle time and increases UPH. The clips come in the reel form and high performance clip singulation system trims them before the high speed bond head system pick them up and attached on the leadframe. Figure 3 is the clip pick up tool or high speed bond head system and Figure 4 is the clips in reel feeding. Figure 5 demonstrates array bonding whereas 6 clips (2x3 arrays) are attached on QFN leadframe at each bond.

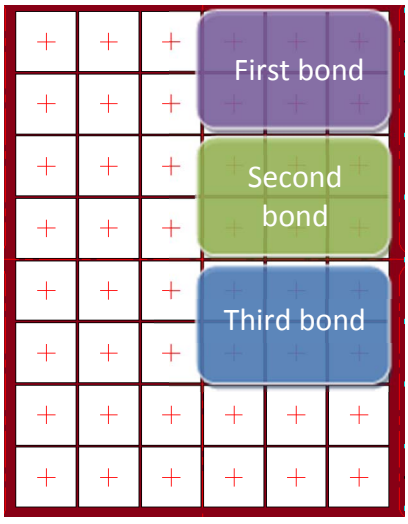


Fig. 5. Clips bonding in 2x3 arrays

One time reflow soldering of Clips and Dies together is a very challenging process especially stacked Dies and Clips configuration with small Dies and Clips were involved. The challenge is that during reflow at solder liquidus temperatures, Dies and Clips are floating in molten solder liquid and they

can be shifted or misaligned after solder reflow as well as solder over-flow if the volume is not optimized. UTAC controls Clip's placement accuracy and able to achieve more than 97% yield even with stacked Clips configuration.

Board Level Thermal Cycling Test Reliability

QFN package offers small package form factor with tight Die to package clearance, reduction of package size compared to leaded package. Increasing die to package ratio poses thermal cycling on board reliability concern since silicon is well-known to be the major source of coefficient of thermal expansion (CTE) mismatch between package and PCB. Higher CTE mismatch will induce higher solder joint stress forcing the joint to fail faster.

QFN 5x5mm with 32 I/O is used as a test vehicle for thermal cycling on board (TCoB) reliability test. The pin to pin pitch is 0.5mm and overall package thickness is 0.85mm. 3.6x3.6mm dummy die is attached at the package center and daisy chain connection is formed by lead to lead bonding with gold wires. Figure 6 shows QFN package daisy chain bonding diagram and package outline drawing.

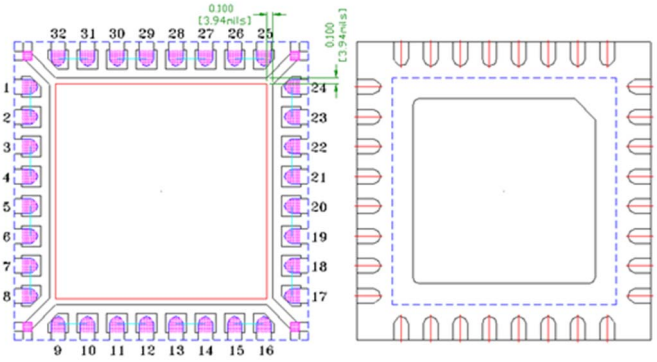


Fig. 6. QFN 5x5mm 32 pins

Thermal cycling test is conducted with 1mm thick PCB fabricated with high Tg FR-4 and 4 copper layers. The PCB is designed such that it will form integrated daisy chain connection with package as per IPC-9701A recommendation. [2] PCB dimension is 200x150mm and 12 daisy chain units were mounted on single sided. Air chamber was used for accelerated temperature cycling range at -40ºC to 125ºC with 15min dwell and 15min ramp, each cycle is 60 minutes. Thermal cycling profile is illustrated in Figure 7.

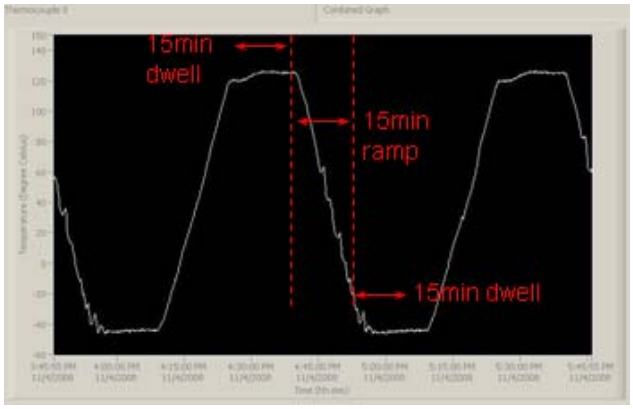


Fig. 7. TCoB thermal cycling profile

Total 48 units were tested until more than 65% of the test samples were failed in order to study characteristic life cycle. The units were in-situ electrical resistance monitored by using event detector and data logger. Failure criterion is 20% increase in nominal resistance for five consecutive readings. Even with the stringent temperature swing of 165 ºC, QFN 5x5mm passed thermal cycle 1,300 cycles without failure. This is robust performance especially with Die length to package length ratio of this device is 72%. Two parameter Weibull plot is showed in Figure 8 and characteristic life is 2,380 cycles. Weibull characteristic life is for 63.2% of failures.

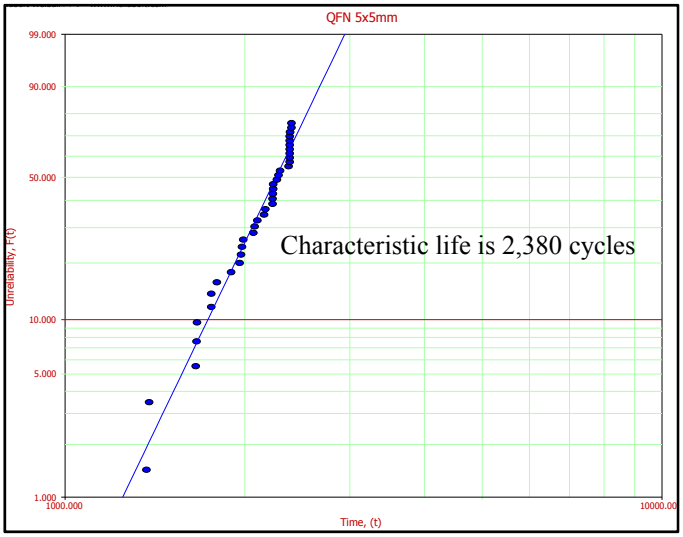


Fig. 8. Weibull plot for TCoB characteristic life

Simulation and reliability modeling

Creep strain energy based fatigue correlation models were studied to analyze the copper clip impact on board level reliability. It has been reported that Wei Sun et al. new curve fitted model can predict QFN solder joint reliability with good accuracy.[3] In this study, Schubert's hyperbolic sine constitutive model [4] is used for lead-free solders and Wei Sun's fatigue correlation model is used for characteristic life

prediction. Schubert's constitutive model is listed in Table 1 and Wei Sun's correlation model in table 2.

Table 1. Constitutive equations and property for lead-free solder [4]

Solder composition	Constitutive equation
Sn3.8Ag0.7Cu Sn3.5Ag0.75Cu Sn3.5Ag0.5Cu (Schubert et al. [16])	$\dot{\varepsilon} = 277984[\sinh(0.02447\sigma)]^{6.41} \times \exp\left(\frac{-6500}{T(^{o}K)}\right)$
E (MPa)	61251-58.5T (degree K) (Schubert et al. [16])
υ	0.36
CTE (ppm/K)	20.0

Table 2: Wei Sun's correlation model for QFN [3]

Acc. Creep Energy Density	$N_{cha} = 741.37 w_{acc}^{(-0.39)}$

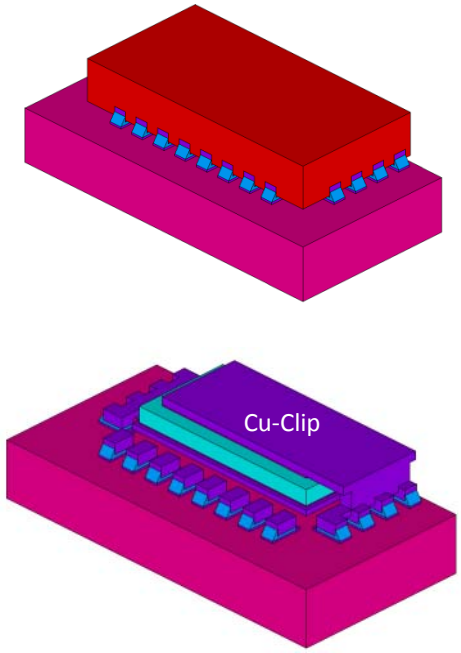


Fig. 9. : FEA model with and without mold compound

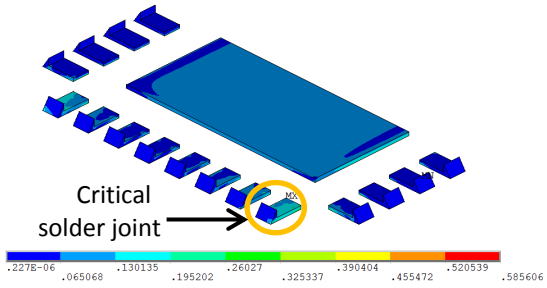


Fig. 10. Accumulated creep energy distribution at solder joints

Table 3 shows the accuracy of creep energy based correlation model with respect to actual test and comparison of characteristic life between standard wirebond QFN and Cu-clip QFN. Both models have same die size, die thickness, material set except leg #1 is using bondwire for connection between Die to lead while leg 2 is using Cu-clip. The impact of adding the 150um thick copper-clip for Die top interconnect on thermal cycling on board reliability is not significant. The study is for solder joint reliability while the device is exposed to temperature swing of at -40ºC to 125ºC but does not include Die's power dissipation effects.

Table 3: TCoB performance of QFN 5x5mm with and without Clip

Leg #	Description	Experiment results (cycles)	Energy-based prediction (cycles)	Accuracy (%)
1	Standard QFN 5x5mm	2,380	2,665	12%
2	QFN 5x5mm with Cu Clip	-	2,615	-

Thermal Performance

Cu-clip contributes to better thermal performance by providing efficient thermal dissipation from Die top to the leadframe. It helps to reduce the maximum junction temperature during operation and extend the device's operation life and reliability.

CFD based thermal analysis were performed to compare device's thermal resistance from Junction to Ambient (Theta JA) under still air environment as per JEDEC standard JESD51-2A. [5] The center Die attach paddle of the package is assumed soldered to a four layers JEDEC PCB (2S2P) PCB with thermal vias connected to M3 layer of the PCB for better heat flow. Thermal study is extended for attachment voids impact on thermal resistance. 30% and 50% of Die's attached solder voids were compared with no voids thermal performance. Power dissipation of the Die is 3.1W and the ambient temperature is 25°C.

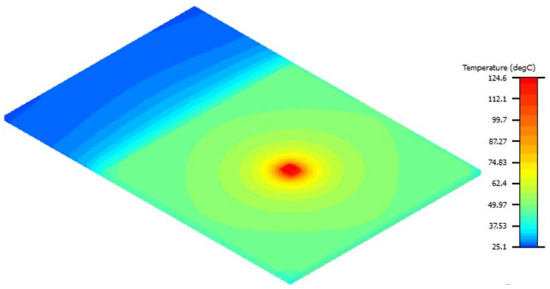
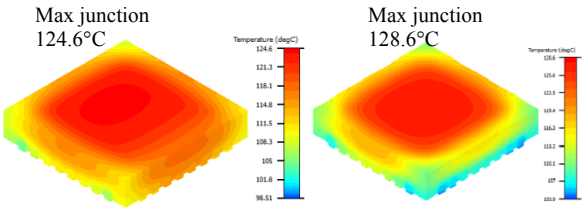
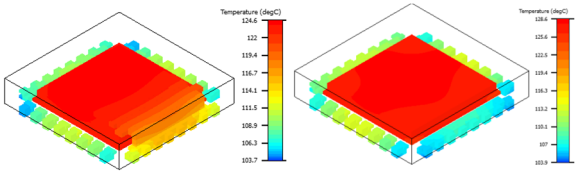


Fig. 11. Thermal distribution of the package with JEDEC 2S2P PCB at still air environment



(a) (b)

Fig. 12. Thermal distribution of the packages
(a) Cu-clip QFN (b) standard QFN without clip



(a) (b)

Fig. 13. Thermal distribution of the packages (mold hidden)
(a) Cu-clip QFN (b) standard QFN without clip

As illustrated in Figure 12, the package with Cu-clip runs 4 degree cooler while consuming the same amount of power 3.1W since the Cu-clip providing additional thermal path on Die top. Most importantly, it can meet the thermal budget of maximum junction temperature < 125 °C. Table 4 shows the comparison of the Die's junction temperature with respect to voids. Thermal performance degrades faster with voids for the package without Cu-clip and cu-clip QFN with 50% voids is cooler than wirebond QFN without voids.

Table 4: Thermal performance of the packages with and without clip and Die attach voids at still air test

		Maximum junction temperature (°C)		
Leg #	Description	No Die attach void	30% voids	50% voids
1	Standard QFN 5x5mm	128.6 (base line)	131.1 (↓2%)	132.9 (↓3%)
2	QFN 5x5mm with Cu Clip	124.6 (base line)	125.7 (↓1%)	126.6 (↓2%)

Die junction to top case thermal resistance (Theta JC-top) is extracted from top cold plate set-up with two layers JEDEC PCB (1S0P). The setup is to allow the majority of the heat to dissipate towards the top case and Theta JC is normally used to determine cooling capacity of the package at mold top surface.

Table 5: Theta JC of the packages with and without clip at top cold plate test

Leg #	Description	Maximum junction temperature (°C)	Theta JC (°C/W)
1	Standard QFN 5x5mm	80.1	17.8 (base line)
2	QFN 5x5mm with Cu Clip	66.2	13.3 (↓25%)

Package with lower thermal resistances will have better thermal performance. Cu-clip reduces thermal resistance from silicon junction to mold top case. When Cu-clip package is combined with a heat sink, more heat can be transferred to the air through nature convection or forced air cooling. It will allow the package to run cooler or draw more power while maintaining maximum junction temperature. Fig. 14. shows Cu-clip QFN with heat sink attached on top of the package for better cooling.

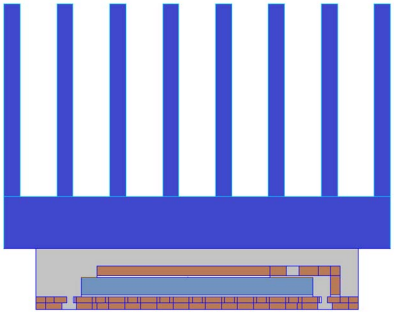


Fig. 14. Cu-clip QFN with heat sink on top

Electrical Performance

Table 6 is the electrical resistance comparison of copper clips and wires. Figure 15 shows the challenge for multiple wires with limitation on wire to wire clearance as well as the clearance to lead edge. Maximum 43 wires are limited by lead's area but the clip has potential to enlarge to cover the bigger Die area to make use of full Die top metallization for lower RDS(on). 43 copper wires with 50um diameter were needed to get similar AC resistance at frequency 100 MHz. Even though comparable AC resistance is achieved, DC resistance is almost two times higher than a single clip.

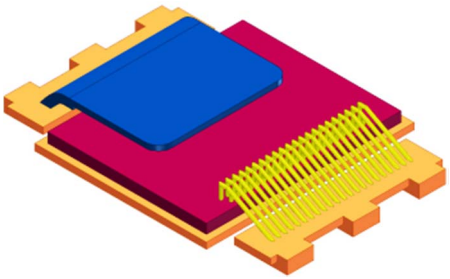


Fig. 15. Copper clip and wires model

Table 6: Electrical resistance comparison

Material	Dimension	DC Resistance (mΩ)	AC Resistance (mΩ)
Copper Wire	50 µm dia x 43 wires	0.19	60
Copper Clip	2.0 x 1.8 x 0.127 mm	0.10	60

Package Level Reliability

Moisture sensitivity level (MSL) test and unbiased accelerated moisture resistance (uHAST) test are designed to qualified package level reliability and classification level of non-hermetic package that are sensitive to moisture-induced stress. Cu-clip QFN packages are qualified for MSL 3 with test condition of 192hours, 30°C/60% RH as per IPC/JEDEC J-STD-020D standard. [6] uHAST is performed to evaluate the reliability of non-hermetic packages in humid environments. It is a highly accelerated test which employs temperature and humidity conditions to accelerate the penetration of moisture to identify package's internal failure mechanisms. The package passed the uHAST at the test condition of 130°C/85% RH at both 96Hrs & 192Hrs as per JESD22-A118A standard. [7] The package reliability test results of one of the Cu-clip packages are summarized in Table 7 below. The package consists of two MOSFETs, one driver Die and two copper clips.

Table 7: Package's Reliability test result of multi-clips QFN

RELIABILITY TEST	DURATION	CONDITION	SS	TEST RESULT
1.MSL-L3 @ 260'C (+5/-0)	192 HRS	30'C/60%RH	154	0/154
2. UHAST-P_L3	96 HRS	130C/85%RH	77	0/77
3. 1 UHAST-P_L3	192 HRS	130C/85%RH	77	0/77
4.TMCL-P_L3	500 CYC	-55/150C	76	0/76
5.1 TMCL-P_L3	1000 CYC	-55/150C	75	0/75
6.HTSL W/O PRECON	150C	504 HRS	77	0/77

Conclusions

Copper Clip QFN package shows advantages over Copper wires with lower electrical impedance (low RDS(on)), better thermal performance and also passed high reliability. Array clips bonding is illustrated in the paper. Wei Sun's correlation model for QFN characteristic life prediction is in good agreement with actual test results. Even though QFN package with Cu-clip shows comparable thermal cycling performance with standard QFN, it has the advantage of lower maximum junction temperature while the device is dissipating the same amount of power. It means Cu-clip QFN will have longer operation life than wire bond package. Cu-Clip QFN also shows more stable thermal performance with minimum increased in Die junction temperature with solder voids. It will allow consistent power dissipation during RDS(on) stage.

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