Comprehensive Modeling of Stress-Strain Behavior for Lead-Free Solder Joints under Board-Level Drop Impact Loading Condition

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Abstract

Board level drop testing is an effective method to characterize the solder joint reliability performance of miniature handheld products. In this study, some drop testing results were summarized based on our previous board-level drop tests. And then the finite element modeling and simulation were conducted to investigate and understand the drop reliability of lead-free solder joints by considering different factors. The strain-rate dependent material properties for lead-free solder has been developed by us and successfully applied in FEA simulation. The important finding of this study is that the constitutive model used has a major impact on dynamic response of solder joint stress and strain results. It was expected that the strain-rate dependent plastic model gave better correlation results than the simple elastic model or bilinear plastic model.

In addition to solder material properties, many other factors, including package locations on the PCB, boundary conditions, input-G level, PCB thickness and solder materials, were also simulated to investigate their effects on stress strain performance of solder joint. Comparing to clamped boundary, the 4-screw support condition leads to higher stress level in solder joint. Higher input G-level results in higher solder stress due to larger inertial force and deflection effects on solder joint. The thinner PCB and softer solder can improve the drop performance of board-level electronic assembly.

1. Introduction

Board-level drop test is an effective method to characterize the solder joint drop reliability performance. JEDEC standard about board-level drop test for components of handheld electronic products provides the guideline for conducting drop reliability performance assessment of electronic assembly. However, it is seems that the specified G level, pulse duration and support condition by JEDEC standard result in fewer drops to failure and other drop loading conditions also should be investigated. Up to date, we have conducted lots of drop impact tests and analyses for both lead-free and SnPb solder jointed electronic assembly [1-5]. The experimental results revealed that drop reliability of electronic components is strongly dependent on input G-level, component location on the PCB, support boundary conditions, solder materials, and influence of different intermetallic compound formation of interface between pad and solder. In this study, the finite element modeling and simulation were conducted to investigate and understand the drop reliability by considering different factors such as component locations on the board, input-G level, support conditions, solder material, etc.

Recently, more FEA simulations were carried out for drop impact reliability study. The dynamic material properties of solder are different from static ones because the dynamic material properties are dependent on strain rate. During a drop test event, dynamic hardening causes the yield stress in the solder to rise several times above the nominal monotonic tensile test yield stress. The solder constitutive model used in FEA simulation will affect stress-strain behavior of solder significantly. In drop impact simulation analysis, the over-simplification of deformation behavior of solder joints (ie: assuming elastic stress criteria) can lead to wrong conclusions in the physics-of-failure understanding in drop impact tests. From existing literatures, many researchers [6-8] just used elastic properties or plastic properties from static tensile test for solder to do the FEA simulation for drop impact reliability evaluation of lead-free solder joints. So, these FEA results are not acceptable to explain the drop failure mechanism. Board-level drop reliability test and analysis require dynamic characterization of high strain-rate properties of solder and solder joint failure tests. The strain-rate material properties for lead-free solder has been developed by us and successfully applied in FEA simulation [3].

In addition to solder material properties, many other factors, including package locations on the PCB, boundary conditions, input-G level, solder materials and PCB thickness, were also simulated to investigate their effects on stress strain performance of solder joint for helping to understand the drop impact failure mechanism of electronic assembly. Comparing to clamped boundary, the 4-screw support condition leads to higher stress level occurred in solder joint, which indicates that support condition by JEDEC standard will induce the faster drop failure due to larger PCB bending and higher output acceleration effects, which is consistent with drop testing results [2]. Higher input G-level results in higher solder stress due to larger inertial force and bending effects on solder joint. Simulation results also reveal that the critical solder joint is located on component corner and the solder/PCB interface has larger stress level than solder/component one, which are verified by experimental result analysis for failure location and failure mode [1]. In order to further quantitatively understand the drop failure mechanism (failure site and mode), more material

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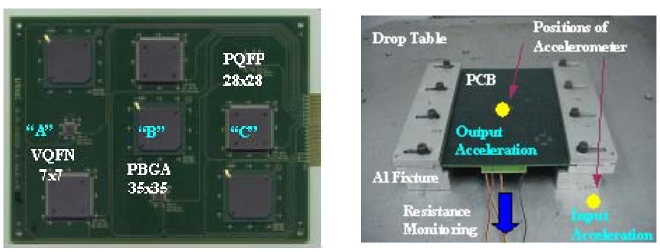
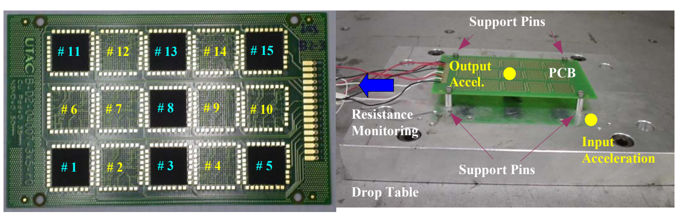
characterization tests are needed to develop the failure criterion for different materials and interfaces.

2. Drop Test and Summary

The details for drop impact test and result analysis can be referred to earlier papers [1-2,4], and a summary is given in this section. The shock test machine was used to provide the drop impact load for board-level specimen with horizontal drop orientation and facedown packages as shown in Fig. 1. Two different specimens were used. Fig .1 (a) shows the drop board with 35x35mm PBGA, 28x28mm PQFP and 7x7mm VQFN mounted on PCB with size of 210x150x1.6mm using clamped-clamped boundary condition along long edges. Fig. 1 (b) shows the 15x15mm FBGA specimen and the test board with size of 132x77x1.0mm follows the JEDEC standard. Two solder compositions of 62Sn36Pb2Ag solder and Sn4Ag0.5Cu solder and two pad surface finishes of ENIG and OSP were used for above two specimens to investigate the effect of solder material and board finish on drop reliability of solder interconnects. Daisy chain was designed for each package and the dynamic resistance measurement system was used to measure the resistance of daisy-chained solder joint to determine the drop to failure [1-2].



a) PBGA, PQFP and VQFN specimens and clamped boundary



b) FBGA specimen and 4-screw support boundary

Fig. 1 PCB specimens and support conditions.

2.1 Drop test with Input-G of 600g

The experiment was performed with an input peak acceleration of about 600g and 2ms duration at the drop table. The output acceleration of PCB center for specimen (a) as shown in Fig. 2 is more than input-G due to PCB bending effect. The result of drop to failure shows that PBGA component is more prone to drop impact failure than PQFP and VQFN components. For PBGA packages, the dominant failure is IMC layer brittle fracture. As for the PQFP packages, failures were not due to solder joint crack but component failure with the lead fingers breaking off from the mold compound due to fatigue of leads. The VQFN components are the most resistant against impact forces among the three components due to its smallest size and mass. Failure data and analysis can be found in details in ref. [1].

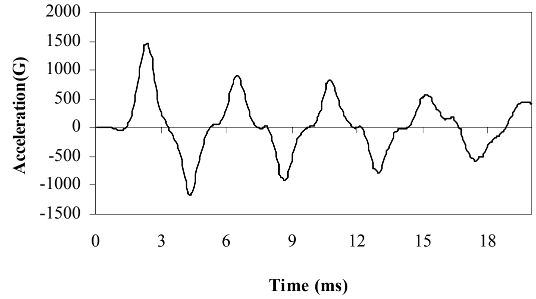


Fig. 2 Output accelerations of PCB center for specimen a.

For FBGA specimen, the averaged drop to failure data was shown in Fig. 3. With board symmetry consideration, the packages are grouped with A, B and C as shown in Fig. 3 in order to get more sample size for analysis. For above two test boards, the drop reliability of the Pb-based specimen is better than the Pb-free specimen regardless of the types of surface finish. The OSP finished test board has better drop performance than ENIG finished test board for both Pb-based and Pb-free specimens. The test results also captured the location dependent failure trend of the solder joints. Packages in group "A" located at the PCB center edge suffered the most drop impact damage due to the large deformation constituted by both the bending and twisting modes. Study by Syed et al [9] revealed similar observation for CSP packages. In their test the PCB is fully populated with fifteen components. The groups "B" and "C" have similar drop reliability for this test board populated with 7 components.

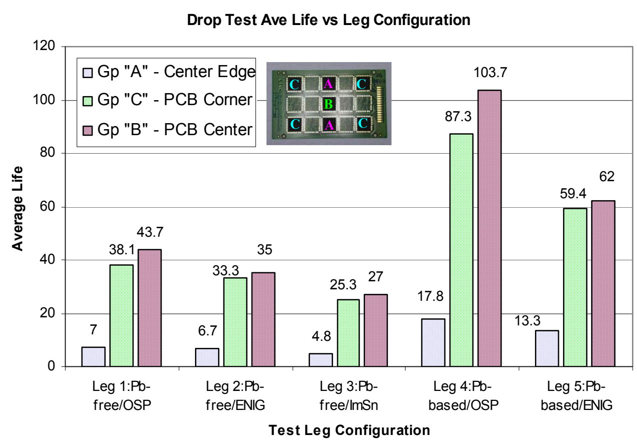
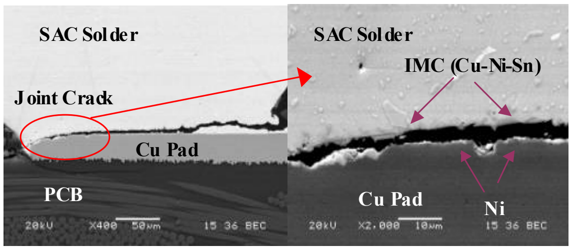
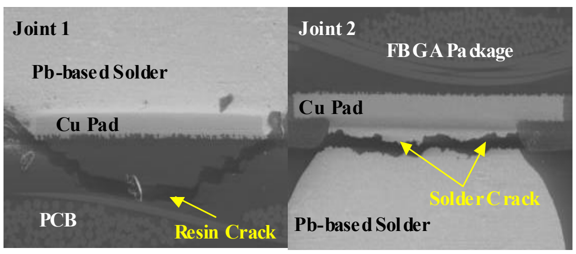


Fig. 3 Drop test failure cycles for different test legs.

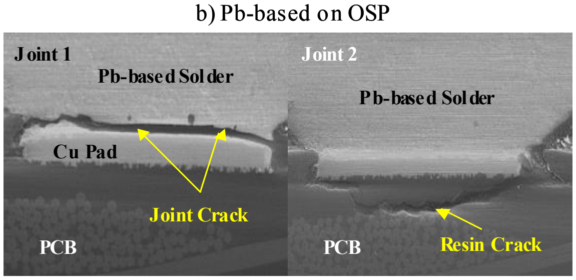
The failure analysis was conducted after test. The results show that the similar failure mode for PBGA and FBGA packages. For lead-free specimen, the dominant failure mode is IMC layer brittle fracture (see Fig. 4 a). For Pb-based specimen, the failure mode can be solder cracking, PCB resin peel off and copper trace broken failure for OSP finish case (see Fig. 4 b); while for ENIG finish case, the failure mode can be IMC brittle fracture and PCB resin peel off (see Fig. 4 c). It can be seen that surface finish and solder alloy affect the drop failure mode significantly. The detailed explanations for failure mode can be found in our papers [1-2,4].



a) Pb-free solder joint failure



b) Pb-based on OSP



c) Pb-based on ENIG

Fig. 4 Different failure modes and sites.

2.2 Drop test with Input-G of 1500g

The drop test was also conducted using JEDEC standard recommended input-G level of 1500g peak acceleration and 0.5ms duration. Fig. 5 shows the result comparison. It can be seen that the drop to failure reduces significantly when input-G level increases from 600g to 1500g. The Pb-based specimen has better drop performance than Pb-free one for two input-G level tests. The input-G level has more significant effect on drop reliability of center edge package with Pb-free solder. Similar failure mode was observed for drop test using different input-G levels.

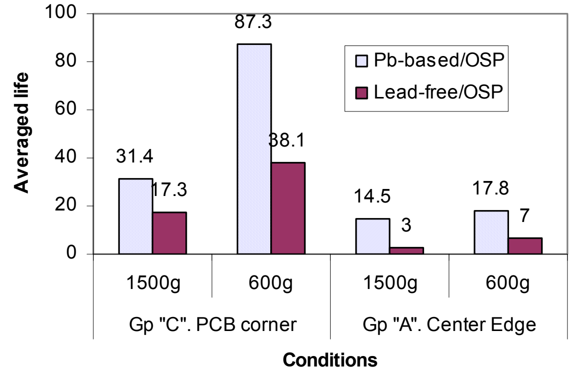


Fig. 5 Drop life comparison for different input-G levels.

3. FE Modeling and Simulation for Drop Test

3.1 FE simulation for PBGA specimen considering different solder constitutive models

In this section, the FE modeling and simulation were performed for PGBA specimen considering solder joint with different constitutive models. The input-G method is an effective and accurate drop simulation method compared to input-D and whole modeling methods [10]. Therefore, input-G method was used for all FE simulations in this study. For convenience, just center PBGA component was simulated. So the model can be replaced by one simple quarter model due to symmetry as shown in Fig. 6. Symmetry boundary conditions were used in the quarter model. The input acceleration from experimental measurement was applied on clamped PCB edge. The fine mesh was implemented for corner critical solder joint with other solder joints having cubic shape and coarse mesh. It was known that damping effect is important for dynamic behavior of PCB under drop impact load. Therefore, calibration study was carried out in FE simulation to achieve optimal damping factor by comparing simulation result and experimental result. The optimal damping ratio of 0.02 was achieved by comparing the output acceleration of PCB center as shown Fig. 7 from simulation result with acceleration as shown in Fig. 2 measured from drop impact.

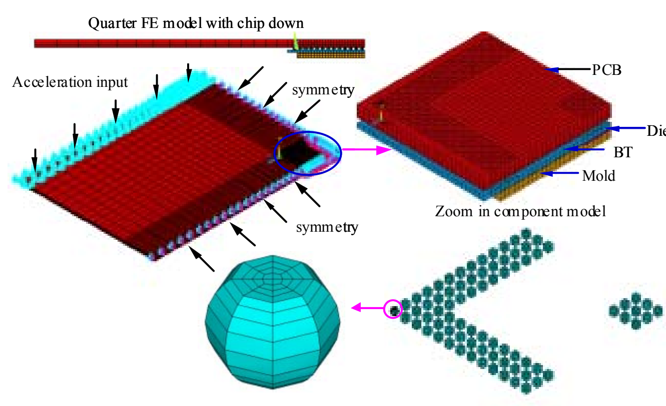


Fig. 6 Quarter FE model for PBGA assembly.

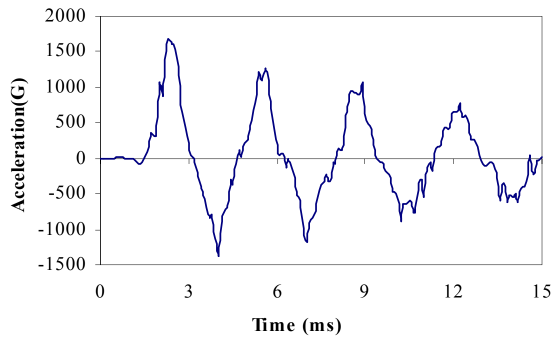


Fig. 7 Acceleration of PCB center from FEA simulation.

Simulation results show that the PCB/solder interface has more stress-strain level than component/solder interface, which is consistent with the failure site from testing. The peel stress peak value is similar to first principle stress peak value, which indicates the peel stress is dominant stress and will be considered as a failure driving force for interface brittle failure [3]. Plastic deformation of solder joint can be expected in dramatically dynamic loading such as drop impact. It is needed to simulate the solder behavior when subjected to drop impact loading using strain rate dependent plastic model. The Young's modulus, yield stress and tangent modulus increase with strain rate increasing. We have developed the strain-rate dependent material properties for SnAgCu solder and successfully implemented them in drop simulation [3]. In this udy, the solder stress comparison was conducted for different solder models such as linear elastic, bilinear plastic and strain-rate dependent. Fig. 8 shows the peel stress of critical node for different solder models. It can be seen that the peak value of peel stress reduces by 50% when considering solder dynamic plastic behavior compared to elastic model. The bilinear plastic model leads to slight lower peak value than strain-rate dependent model. It is expected that the solder suffers different strain rate under impact loading and the strain-ate dependent model is suitable to simulate the solder behavior when subjected to drop impact loading.

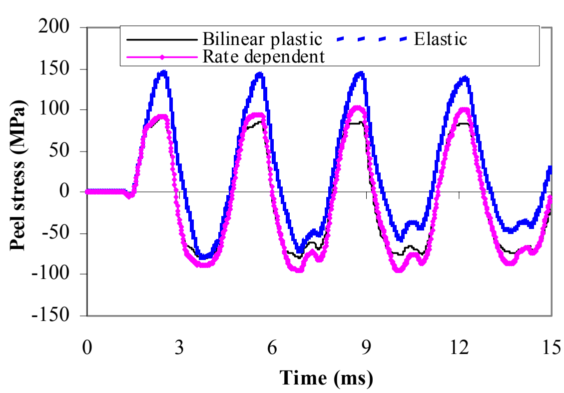


Fig. 8 Peel stress comparison for different solder models.

__3.2 Location dependent FE simulation analysis for FBGA specimen__

Finite element modeling and simulation of the FBGA assembly (specimen b) with Pb-free solder was performed to investigate location effect on dynamic response of package during drop impact. Assumption was made that the first vibration mode is dominant for the FBGA specimen subjected to drop impact load. Therefore, a quarter model was used in this study with symmetric boundary conditions prescribed as shown in Fig. 9. Comparing the FE model in Fig. 9 with specimen shown in Fig. 1, the full package model for #1 FBGA, half package model for #3 FBGA and quarter package model for #8 FBGA were simulated. The materials considered in FE simulation include FR4 PCB, solder, copper pads on both the board and package sides, BT substrate, silicon die and mold compound. The input acceleration from experimental measurement with peak acceleration of 600g and 2ms duration was applied onto the PCB screw support location. Strain-rate dependent material properties of the SnAgCu solder were implemented in the FE models and simulation [3]. In the simulation, the y coordinate refers to vertical drop direction, x along PCB longitudinal (longer) edge, and z along the PCB transverse edge.

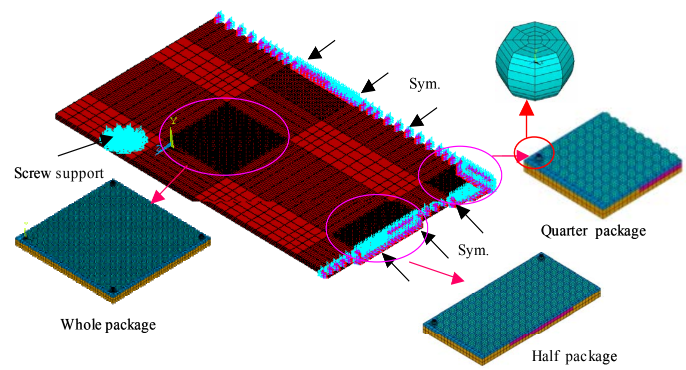


Fig. 9 3D Quarter FE Model for the FBGA Specimen.

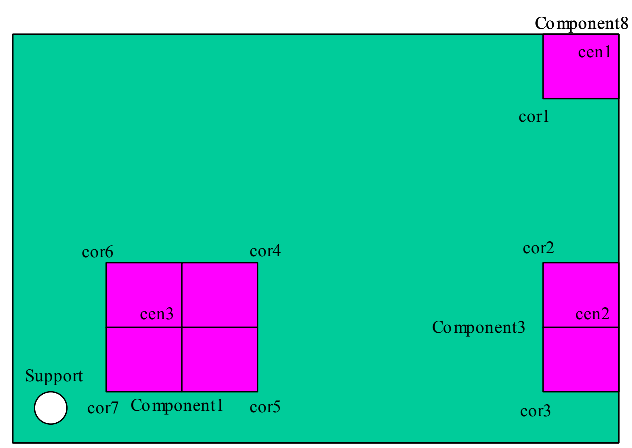


Fig. 10 Schematic for different node locations in FE model.

In order to explain the location dependent results, some markers are defined as shown in Fig. 10. In Fig. 10, the "cen#" and "cor#" refer to the center and corner positions located on PCB side without component when analyzing the

PCB strain or acceleration results, respectively, while the "cor#" refer to the critical nodes of each solder located at outermost corner position of each component when analyzing the solder stress or strain results.

The accelerations of different locations on the PCB are shown in Fig. 11. The FE simulation results illustrate that the acceleration is location dependent and the PCB maximum acceleration occurs at the center of PCB due to larger transmissibility ("cen1" in Fig. 11). The acceleration increases with the distance from screw support to measured position. The position of "cor7" has a similar value to input G-level of the drop table because it is close to the support pin. Therefore, the solder joints of the center package will experience a larger inertial force compared to joints of the corner packages. The strain results along PCB longitudinal direction for different PCB locations are shown in Fig. 12 and some findings are achieved. The strain of corner location is higher than that of center location for each package due to local stiffening effect of component. For each component location, the critical longitudinal strain value occurs at the corner close to the support or free edge. The position "cor7" of the corner package has the maximum strain compared to others.

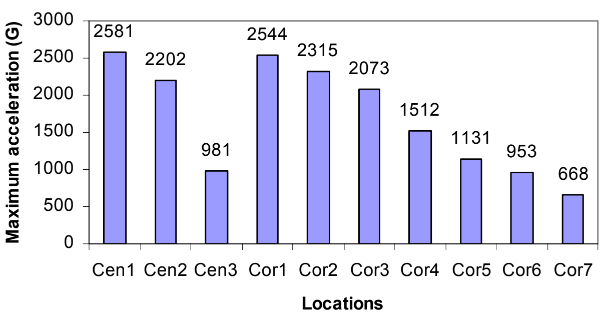


Fig 11 Maximum acceleration of different PCB locations.

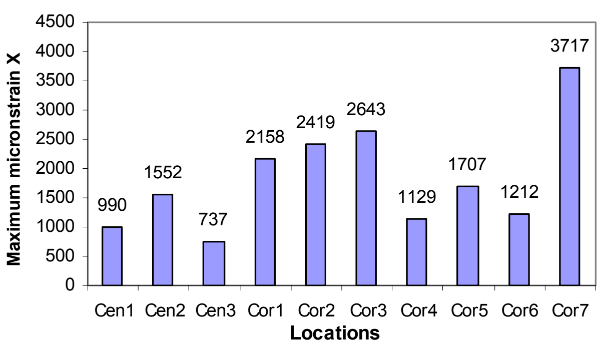


Fig. 12 Maximum strain of PCB different locations.

The solder joint stresses were analyzed as well. The FE results show that the stress level of PCB/solder interface is higher than that of substrate/solder interface, thus solder joint stresses were extracted from the critical node of solder/PCB interface. Fig. 13 shows the maximum peel stress of critical node of solder joint at different locations. It is found that "cor3" has the highest peel stress compared to others, indicating that a joint failure will occur earlier in that location. The stress level of "cor1" is slightly lower than that of "cor7", which helps to explain the observation of group "B" exhibited slightly better drop reliability than group of "C". The critical solder joint for each component can be deduced from Fig. 13: "cor1" for component 8, "cor3" for component 3 and "cor7" for component 1, which are in correlation with experimental finding of failure distribution [2]. The solder stresses obtained from FE simulations can helps to explain the failure mechanism and site observed and is consistent with experimental findings.

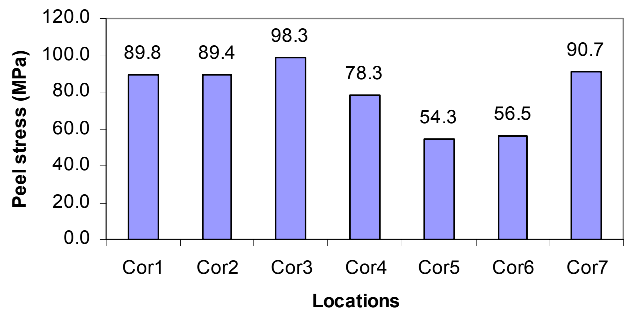


Fig. 13. Maximum peel stress at different solder locations.

3.3 Boundary condition and input-G effect

It was expected that the support boundary for drop test board and input-G level have dominant effect on dynamic response and drop performance of tested assembly. In this section, the FE simulation was conducted for FBGA specimen to investigate these effects. For convenience, just center FBGA package was modeled for comparison. Fig. 14 shows the quarter FE models for different boundary supports such as 4-screw support, clamped two shorter edges, and clamped two longer edges. In the FE analysis of boundary condition effect, the input-G of 600g was chosen as loading condition. Fig. 15 shows the PCB center deflection history comparison for different boundary condition models. Some findings can be achieved from Fig. 15. Firstly, the 4-screw support condition results in the largest bending effect compared to two clamped boundary conditions. Secondly, the frequency of PCB bending is highest for the model with clamping longer edges, which is consistent with modal analysis from that the highest natural frequency was obtained for the model with long edge clamped. Finally, the first bending down deflection has the maximum displacement value during drop impact, and then the vibration displacement reduces due to the damping effect. Based on above analysis, one optimal method for promoting drop performance of electronic assembly is to improve the support boundary of PCB, for example, boundary condition with more constrain can provide better drop reliability of electronics.

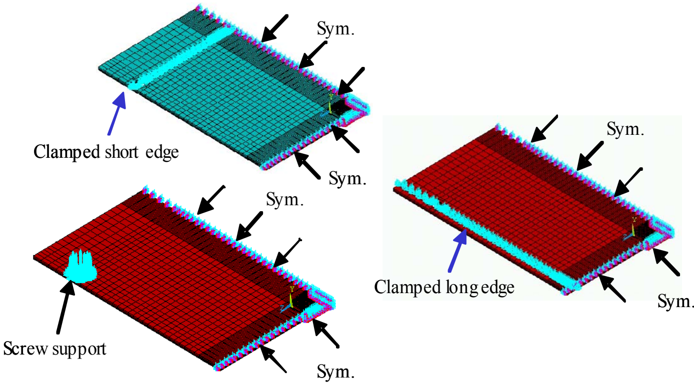


Fig. 14 Three different support boundary models.

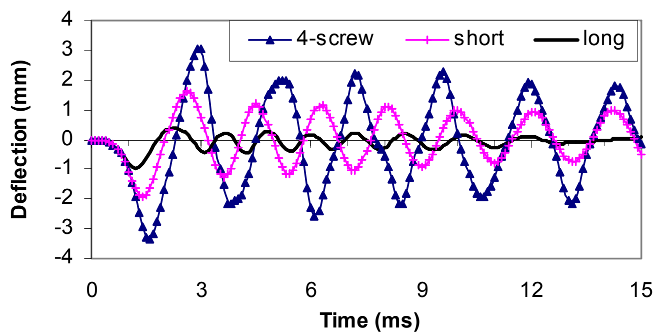


Fig. 15 Deflection history of PCB center for different boundary conditions.

In order to further understand the boundary and input-G effect on dynamic response of PCB assembly, the output acceleration and stress-strain behavior were also extracted. Fig. 16 shows the peak acceleration of PCB center from drop simulation results. The output acceleration of PCB center is higher than input-G level for each case. The output acceleration of PCB center increases with input-G for the same boundary condition. For the same input-G level simulation, 4-screw support boundary results in the highest output acceleration of PCB center compared to clamped support cases, which has the similar trend as the deflection mentioned above. The maximum PCB strain occurs at the PCB position (without component side) corresponding to the component corner. The underneath solder joint is usually critical solder joint with first failure happening site. Fig. 17 shows the maximum PCB strain along PCB length direction. The 4-screw support also results in the highest PCB strain compared to clamped cases. PCB strain increases with input-G level, but the input-G effect on PCB strain is not so significant as that effect on output PCB acceleration.

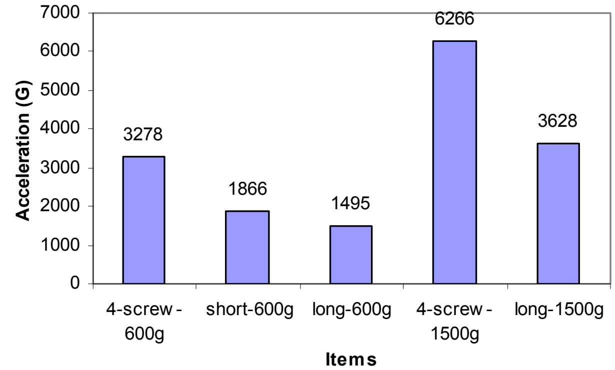


Fig 16 Peak acceleration of PCB center.

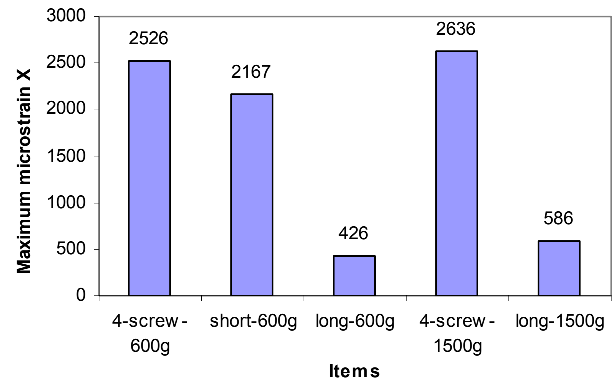


Fig 17 Maximum PCB longitudinal strain.

It was known from test and simulation results that the cornermost solder joint is the critical one and the stress level of PCB/interface is higher than that of component/solder interface [4-6]. In this study, the stress level for the PCB/solder interface of corner solder joint was extracted for analysis. Fig. 18 shows the PCB/solder interface layer nodal number and nodal peel stress of interface perimeter for different support boundary with the same input-G of 600g. It can be seen that 4-screw support results in higher stress level than clamped cases. The crack initial site is found to be located the interface site close to the support position or clamped edges. Fig. 19 shows the normalized peel stress level comparison of critical interface node for different testing conditions with considering peak peel stress as unity for the simulation case of 4-screw support/input-G of 600g. For the same 4-screw support condition, the stress increases by 40% when changing input-G from 600g to 1500g, which provides the reason why higher input-G leads to less drops to failure in drop test as shown in Fig. 5. The clamped boundary condition can help to improve the drop performance because such support condition reduces the interface peel stress compared to 4-screw support case.

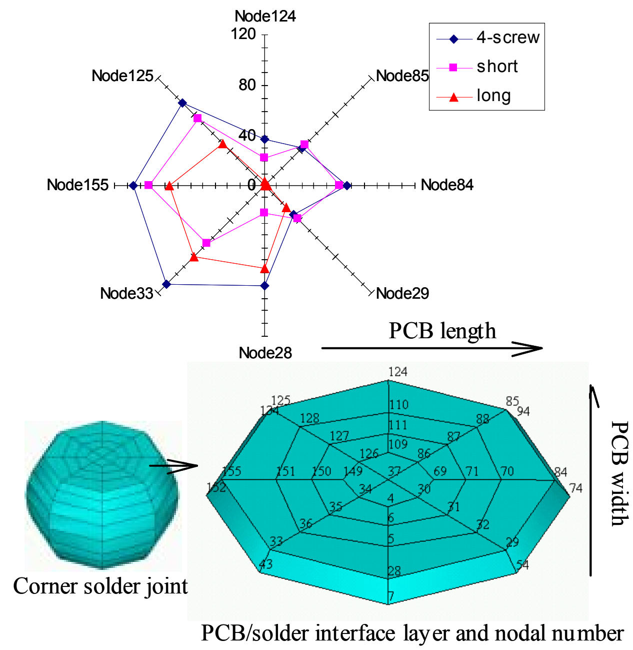


Fig. 18 Nodal peel stress of solder/PCB interface perimeter.

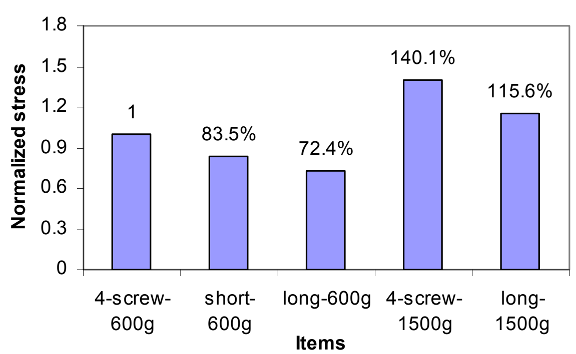


Fig. 19 Boundary and input-G effect on peak peel stress.

Fig. 20. shows the peel strain rate of critical node at PCB/solder interface for different boundary conditions and input-G levels. It can be seen that the solder strain rate drops the rate range from 10^0 to 10^2 for drop impact loading, which has the significant difference with that of solder joint under thermal cycling loading (usually rate from 10^{-5} to 10^{-3}). The yield stress of solder material would increase by 3 times when strain rate increases from 10^{-5} to 10^2, so the rate dependent solder material properties are necessary to do the drop simulation for electronic assembly. Currently, it is still a challenge to get accurate solder material properties under strain rate from 10^0 to 10^2.

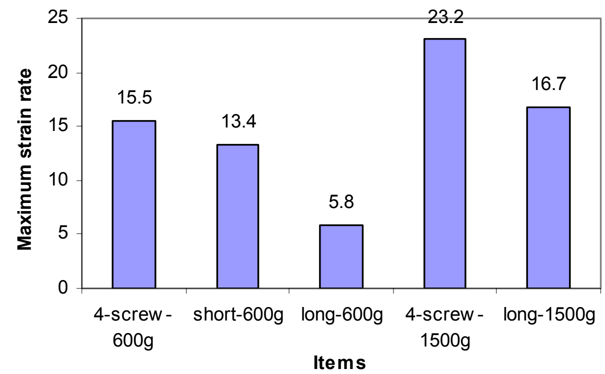


Fig. 20 Peel strain rate of critical interface location.

3.4 PCB thickness effect

The PCB thickness effect on dynamic response and solder stress were carried out here using numerical method. The FBGA assembly in above FE model has the PCB thickness of 1mm. The PCB thickness of 1.6mm was also simulated for FBGA assembly for comparison study. Fig. 21 shows the drop simulation results for both models with different PCB thicknesses. For convenience, the unity were assigned for simulation results from thin PCB model (1mm thickness), such as PCB center acceleration, PCB center deflection, PCB strain at component corner and solder peak peel stress. The PCB center acceleration and deflection, PCB longitudinal strain is higher for thin PCB model compared to thick PCB case. The thinner board is more compliant, and therefore the larger board deformation become easier, which will induce larger PCB deflection and strain. However, the peel stress of solder/PCB interface is higher for thicker PCB model. Therefore, the drop performance is worse for thicker board specimen, which has the similar trend as that the thicker board has lower thermal fatigue life [11].

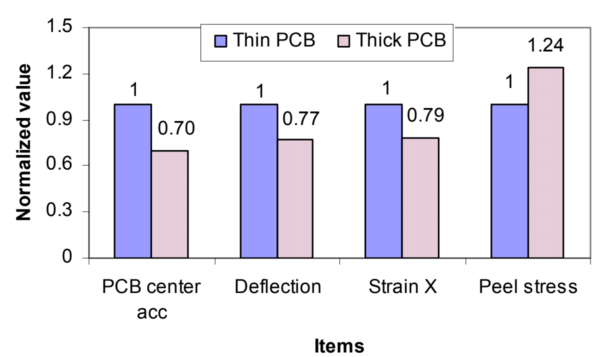


Fig. 21 PCB thickness effect on dynamic response.

The PCB thickness effect on acceleration and solder stress has the inverse trend from simulation results as shown in Fig. 21. In ref. [12], it was also found that the maximum acceleration and the maximum dynamic stress are affected differently by different factors by analyzing beam structure element. The recommendation is that the maximum stress, not the maximum acceleration, should be used when comparing the dynamic strength of electronic assembly.

3.5 Pb-free vs. Pb-based solder

Many drop experiments showed that the Pb-based assembly has the better drop performance than Pb-free assembly [1-2,4,7,13]. Simulation results reveals that the peel stress of critical solder joint is higher for SnAgCu soldered assembly as shown in Fig. 22, which can help to explain why the Pb-free soldered specimen is prone to drop failure compared to Pb-based specimen. Usually, the SnAgCu solder has higher modulus and yield stress than SnPb solder, so the higher stress level occurs in the solder/PCB interface for SnAgCu soldered specimen. For the same IMC composition, for example, Cu_6Sn_5 for SnPb and SnAgCu solders on OSP finished board cases, the higher peel stress can easily induce the IMC brittle failure. Therefore, the softer solder joint (Pb-based) is better than harder solder joint (Pb-free) in terms of drop reliability.

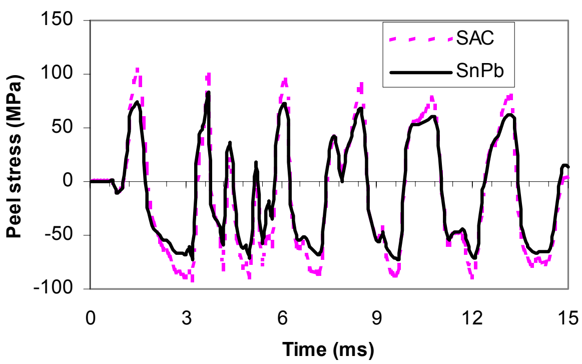


Fig. 22 Peel stress history of critical node for different solder materials.

4. Conclusions

Drop test and simulation were conducted for both Pb-based and Pb-free soldered assemblies. Experimental and simulation results show that Pb-free soldered assembly is prone to failure than Pb-based one. Strain-rate dependent plastic model for Pb-free solder is a suitable constitutive model when simulate the solder stress behavior when subjected to drop impact loading. Location dependent drop reliability was observed from test and verified by FE drop simulation results. Simple 4-screw support induces higher solder stress level and thus reduces the drop performance of tested electronic assembly compared to clamped boundary condition. The drop to failure decreases with increasing input-G level. Thicker PCB will reduce the drop performance of board-level assembly.

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