Analysis of Electromagnetic Susceptibility on High Speed Circuits Located in a Shielded Enclosure

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Abstract — **This paper presents the investigation of the electromagnetic susceptibility (EMS) characteristics of high speed circuit and interconnects located in a shielded enclosure which is connected to an external signal cable. An integrated method is proposed based on full wave electromagnetic analysis combined with high speed circuits modeling in order to exploit the advantages of both techniques in computational efficiency and accuracy for system level EMS problem.**

I. INTRODUCTION

The continual increasing in high speed and high density electronic and electrical systems leads to the electromagnetic susceptibility (EMS) threats of high speed micro-scale and nano-scale electronic devices with various types of electromagnetic interference. In general, sensitive electronic devices are covered by a metallic shielding enclosure in order to minimize the susceptibility and emission problems. However, the integrity of shielding enclosures is often compromised by the apertures and slots which are used to accommodate visibility, ventilation or access to interior components and external cables which are used to pass the signal or power to the internal circuitry [1]. Such openings allow exterior electric and magnetic field to radiated from or penetrate into the internal sensitive equipments. This paper is concentrated on this scenario.

Considerable work has been done on the electromagnetic characteristics of the shielded electronic devices based on the shielding effectiveness evaluation. Analytical or semi-analytical techniques provide a closed-form solution, allowing for fast calculations, but are limited to cases with simple geometries [2]. The significant advances in computing power and computational electromagnetic techniques in recent year, it is practical to analyze the problem based on the full wave analysis [3]. However, current high speed circuits are very complex. It may be multilayer PCBs consists of many high speed components, IC packages, frequency dependent interconnects etc. Hence, full wave analysis alone may take extremely time and memory consumption. On the other hand, circuit model can give accurate results and widely use in analysis of high speed circuit. As consequences, an integrated method is proposed here based on full wave analysis combined with high speed circuits modeling in order to exploit the advantages of both techniques in computational efficiency and accuracy for system level EMS problems.

In general, high speed circuits are analyzed by transistor level modeling technique and behaviour modeling technique. Transistor level modeling is the actual physical design of the high speed chip or circuit with all accompanied parasitic and a primary method for analysis and design of high speed circuit. However, transistor level modeling is usually complex, especially, when the functionality of the circuit increases and the number of transistors increase. Current high speed circuits can have more than one billion transistors. Usually the simulation of such IC packages may take a lot of time, since the analysis will process the state of every single transistor [4]. In addition, the circuit level description is difficult to obtain from the IC vendor due to issues with intellectual property (IP). To improve the simulation time while protecting IP, the concept of IBIS (Input-Output Buffer Information Specification) behaviour model was introduced by Intel back in 1990s. IBIS model deals with the behaviour of the circuit when various input/output conditions are encountered. The critical electrical characteristics are based on derivative information which are derived by simulation or measurement. Since IBIS is behavioral, the simulation time for a model can run faster than a transistor level model. IBIS does not have non-convergence issues such as encountered in transistor models and can run most industry wide platforms since most EDA vendors support the IBIS specification. In this work, IBIS model is used to analyze the high speed internal circuitry. High speed IC components are connected together via copper traces on the PCB. The ability to predict accurately PCB performance allows designers to integrate high speed circuits into their product and improve system quality and reliability. The waveform quality and the timing margins are adversely affected by high frequency interconnect analog effects such as reflection, dispersion, cross talk, ground bounce and propagation delay. Therefore, an accurate modeling of system interconnects is an important issue in both EMC/EMS and signal integrity analysis. In this work, a frequency dependent lossy transmission line model based on Telegrapher's equations is used to model the system interconnects.

II. MODELING TECHNIQUE

Susceptibility characteristics of high speed circuit inside the shielded enclosure connected with signal cable

is analyzed in this paper. Problem domain is decomposed into two parts: (1) shielded enclosure and signal/cable (2) internal high speed circuit. The schematic diagram of problem domain is shown in Fig. 1. The enclosure is assumed to be PEC. The external shielded enclosure and signal cable affected by the plane wave EMI is simulated using the mixed-potential electric field integral equation technique (MPIE) via the method of moment (MoM). From that simulation, ***the equivalent source model*** is extracted using circuit theory. Procedures are as follows:

Step I: Induced current at the joint point of the enclosure with a signal cable is evaluated by MoM. According to the Norton Theorem, calculated induced current at joint point is treated as the short circuit current source (I_{sc}) in the equivalent source model.

Step II: A delta voltage (V_{delta}) is applied to the joint point and computed the induced current ($I_{jo\,\mathrm{int}}$) at this point by using MoM solver again. Equivalent impedance Z_{eq} is calculated by $Z_{eq} = \frac{V_{delta}}{I_{jo\,\mathrm{int}}}$ (1)

The schematic diagram of the enclosure and equivalent circuit source model are shown in Fig. 2, where Z_T is determined by the way that the cable is connected to the internal circuits and Z_c accounts for leakage impedance to ground depending on the way how the cable is connected to the enclosure. The equivalent source model can easily extend to the multiple cables as the same way. Although it is needed to simulate the MoM simulation two times in order to extract the equivalent source model, the same impedance matrix is required to develop for different apply sources. In the MoM simulation, the most efforts are on filling the elements of the impedance matrix and LU decomposition of that matrix.

Step III: Extracted equivalent source model is used as an input noise source for internal high speed circuit. In this work, four layered PCB with 12 traces and three IC die placed at the top layer of the PCB is considered as an internal circuit to analyze. Internal IC package is modeled using non-linear analog behaviour modeling based on IBIS format and system interconnects are simulated by transmission line model based on Telegrapher's equations.

A. MoM Formulation for Shielded Enclosure and Signal Cable

Let 'S' be the surface of arbitrary combined PEC enclosures and wires illuminated by applied electromagnetic wave, $\vec{E}^i$. The boundary conditions require the total tangential electric field on the conducting surface to be zero,

$$\vec{E}^s(\vec{J}) + \vec{E}^i\,|_{\tan} = 0 \qquad \text{on S} \tag{2}$$

where $\vec{E}^s(\vec{J})$ is the scattered field due to the induced current $\vec{J}$ and $\vec{E}^i$ is the incident electric field. Again, scattered field can be written in terms of the magnetic vector potential $\vec{A}$ and electric vector potential ϕ as

$$\vec{E}^s(\vec{J}) = -j\omega\vec{A}(\vec{r}) - \nabla\phi(\vec{r}) \tag{3}$$

Substitute equation (3) to (2), we get

$$\vec{E}^i_{\tan}(\vec{r}) = j\omega\vec{A}(\vec{r}) + \nabla\phi(\vec{r})\Big|_{\tan} \qquad \vec{r} \in S \tag{4}$$

where $\vec{A}(\vec{r}) = \mu\int_s \frac{\vec{J}(\vec{r}')}{4\pi R} e^{-jkR} dS'$ and

$\phi(\vec{r}) = -\frac{1}{j\omega\varepsilon}\int_S \frac{\nabla'\cdot\vec{J}(\vec{r}')}{4\pi R} e^{-jkR} dS'$.

The equation (4) is solved by using MoM. Galerkin's method is used to derive the linear system of equations. LU decomposition is used to solve the global system of equations.

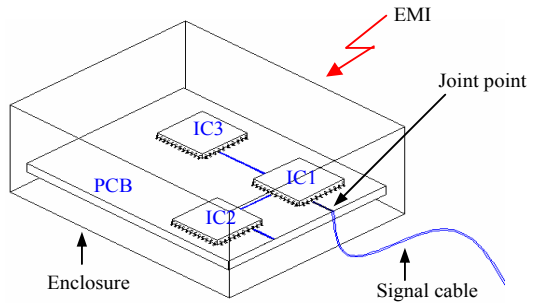

Fig. 1 Schematic diagram of problem domain

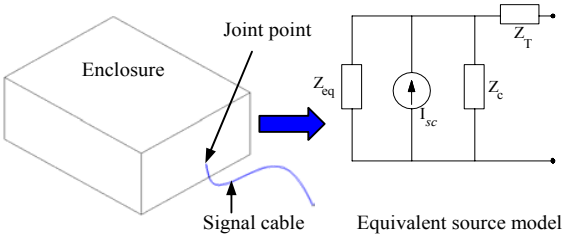

Fig.2 Equivalent source model

B. Modeling of IC with IBIS Model

IBIS specifies a standard form for presentation of information in ASCII format in special files. This information describes behaviour of various input/output buffers that send electrical signals outside the silicon chip or receive such signals. IBIS basically relies on V-I (voltage-current) and V-T (voltage-time) curves or table representing the behaviour of the chip model and also includes timing characteristics, package information and the various parasitic of input/output. This approach is designed to provide model that reveals no proprietary

information about the design or process technology. IBIS format buffer information can be freely downloaded from the internet at the manufacturer websites such as Intel, Motorola, AMD, Hitachi etc.

III. Analysis and Results

Electromagnetic susceptibility characteristic of the high speed circuit inside the shielded enclosure connected with a signal/power cable has been analyzed using the proposed methodologies. Simulation model includes (1) a metal enclosure (20 x 15 x 10 cm) and it is assumed to be PEC, (2) a thin wire signal cable which is directly connected to the internal PCB through the shielded enclosure and (3) four layers PCB and IC die (IC1, IC2 and IC3) which are accommodated in the metal enclosure. Intel bridge chipset 82374EB is used as a simulation example IC package for this work. The IC die is modeled as an array of input and output buffers. PCB has three signal layers with four traces at each layer. All of the copper traces have rectangular cross-section with (w x h = 0.4 mm x 0.06 mm). The segregation distance *s* between the two traces in the same layer is 1 mm. The thickness *d* of each layer is 0.2 mm. Three dielectric media are sandwiched between layers and have the dielectric constant of 2.1, 2.2 and 2.3 respectively. One end of the trace 11 is electrically connected to the external unshielded signal cable and the other end is connected with the IC1 input buffer 1 (Model: ES777700). Therefore, external EMI is directly conducted from the unshielded signal cable to the trace 11 and affected to the IC1 input buffer 1. Output pin of the IC1 input buffer 1 is connected with the IC3 input buffer (Model: ES77700V) through the trace T1. Trace 9 is connected with the IC2 tristate buffer (Model: ES060613) which is connected with another IC1 input buffer 2 through the trace T2. The schematic diagram of the cross-section of the PCB and connections of traces with ICs are shown in Fig. 3 and Fig. 4.

Electromagnetic magnetic interference is considered as a plane wave and it is illuminated to the outer surface of the enclosure and external cable. Induced current at the joint point where the cable is connected with the enclosure is calculated by the MoM. Results are shown in Fig.5. Induced current is the short circuit current source for the equivalent source model. Simulated equivalent source is the input noise source for multi-layered PCB. The electromagnetic characteristic of the PCB traces are solved by the transmission line model based on the Telegrapher's equations. Star-Hspice W element Field solver model [5] is used to solve the transmission line characteristic of the PCB traces in this work. Fig. 6 shows induced noise voltages at the end of the PCB traces. It is found that induced voltage at trace 11 is the most severe case because it is directly connected with the unshielded signal cable. To evaluate the effects of different termination conditions in the traces, five different loads are connected between the ends of the trace 9 and trace 11. Results are shown in Fig.7 and Fig.8. It is observed that different terminations induced different noise voltages on the respective traces and the magnitude of the induced noise voltages are increased while the magnitudes of the load resistances are increased. In addition, the magnitudes of the induced noise voltages depend on the operating frequency.

Since the other ends of the trace 11 is connected with the IC1 input buffer 1 as shown in Fig. 4, conducted EMI along the trace 11 is affected to the IC1. Again, affected output signal of IC1 input buffer 1 is transmitted to the IC3 input buffer through trace T1. Susceptibility characteristics of the IC1 and IC3 input buffers are simulated by IBIS models and shown in Fig. 9 and Fig.10. Similarly, the other end of the trace 9 is connected with the IC2 tristate buffer and the output signal is transmitted into the IC1 input buffer 2 through trace T2. Simulated result by using IBIS models is shown in Fig. 11. It is found that because of the noise voltages induced along the trace 9 and 11, both IC1 and IC2 buffers are operated in malfunctions and it will be affected to the other logic circuits connected with these two IC die.

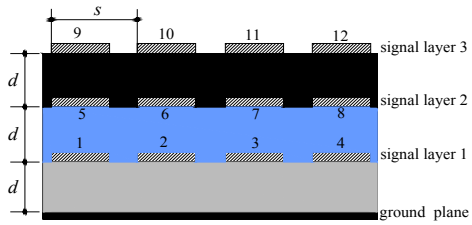

Fig. 3 Cross-section of the PCB

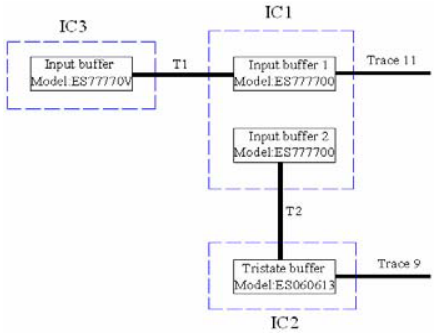

Fig. 4 Schematic diagram of traces connection with ICs

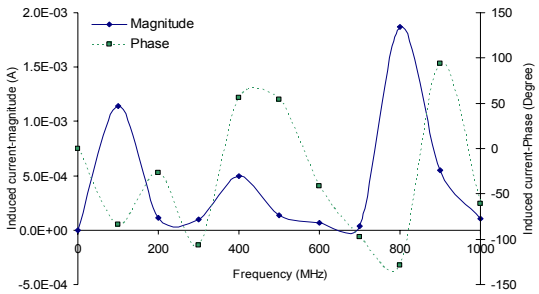

Fig.5 Induced current at joint point

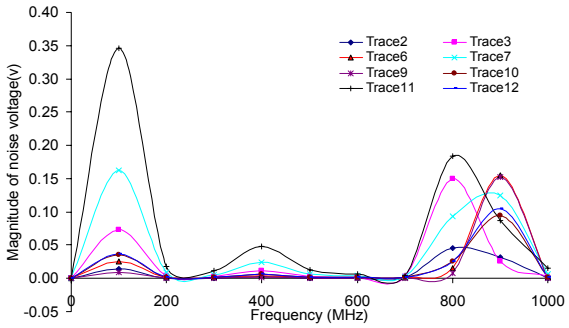

Fig. 6 Induced noise voltages at the end of the different traces

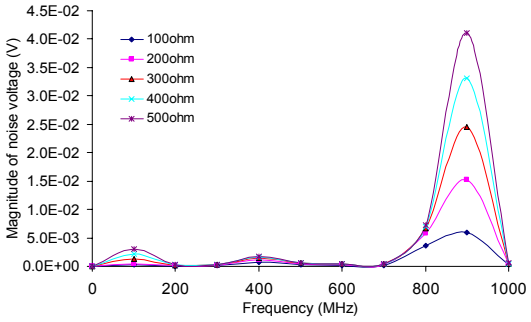

Fig. 7 Induced noise voltages at the end of trace 9 with different terminations

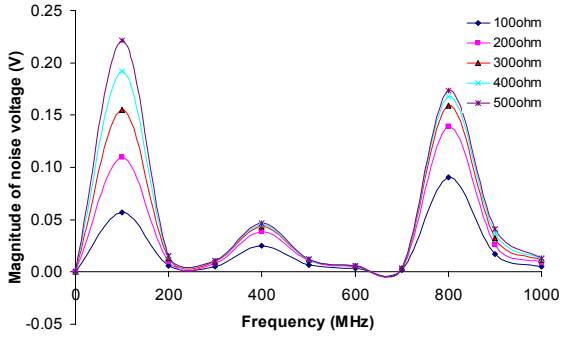

Fig. 8 Induced noise voltages at the end of trace 11 with different terminations

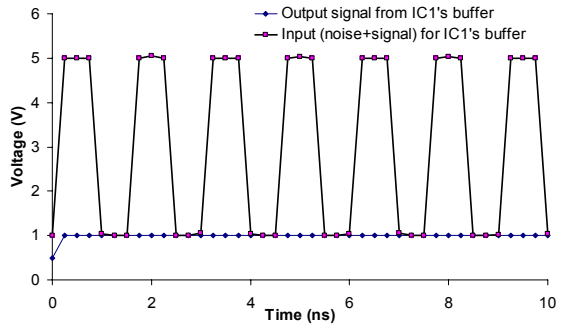

Fig.9 Results from the IBIS model of IC1 input buffer 1 where input is noise+ signal

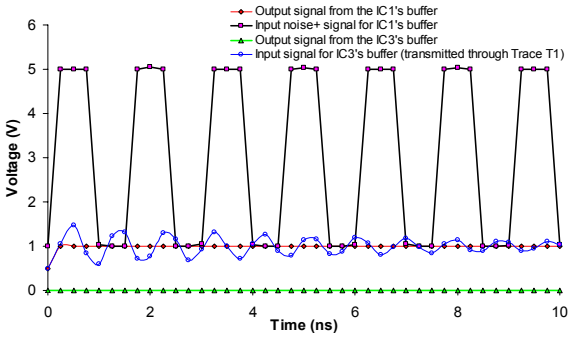

Fig. 10 Susceptibility characteristics of IC1 and IC3 buffers

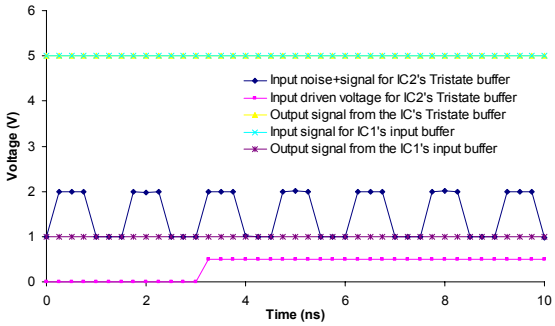

Fig. 11 Susceptibility characteristics of IC1 and IC2 buffers

IV. Conclusions

An improved model of MoM combined with circuit based SPICE solver is presented to analyze the shielded high speed circuit inside a metal enclosure connected to an external wire. Results show that this is an efficient systematic approach for the analysis of the system level electromagnetic susceptibility problem, typically for the shielded device with an aperture/slots, signal/power cable and internal electronic circuits.

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