Design and Development of Stacked Die Technology Solutions for Memory Packages

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Abstract

With the demand in increased functionality for consumer electronics and the need for form factor reduction, stacked die packages have gained its popularity over the recent years. The most efficient way to increase a memory package's capacity without increasing its size is to adopt a die stacking structure. This paper presents three innovative package technologies for DRAM memory packages, with the option of die stacking structures of D2i/D2-wCSP (window Chip Scale Package), D2-FBGA and 2DD2-wCSP. Upfront design considerations such as package structure, electrical performance and board level reliability are discussed. Customised assembly processes are developed for each package type, with full package level reliability qualification. Each package design demonstrated its unique advantages and careful selection of a packaging solution is necessary in meeting individual customer's specific requirements.

1. Introduction

The window Chip Scale Package (wCSP) is a unique package structure for DRAM application where the wirebond pads are located at the chip centerline, as shown in Fig.1 [1]. The active die surface is facing downwards, with the wires bonded in a reverse manner through a channel opening (termed as window) at the center of the substrate. For die stacking, the wCSP stacked die structure will be different compared to conventional packages. For a 2-die stacked, the active side of the top and bottom dies will face upwards and downwards respectively (shown in Fig. 2). Under UTAC's naming convention, this package configuration is termed as D2i-wCSP, where 'i' represents the interposers. The interposers facilitate the bridging of interconnection from the center of the die to substrate, avoiding long wire bonding requirement. In the event when die size, bond pads layout or package size is allowed, it is possible to remove the interposers from the top die for direct wire bonding of interconnection between the top die and the substrate. Fig. 3 illustrates the direct wire bonding concept of the D2-wCSP structure.

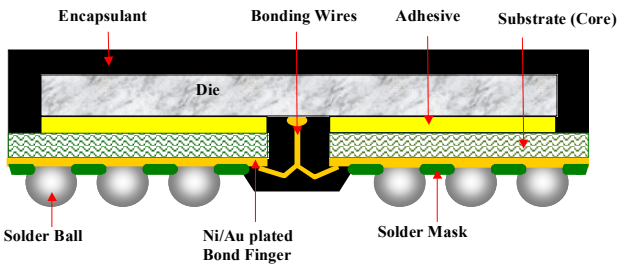


Fig. 1. Typical wCSP Structure.

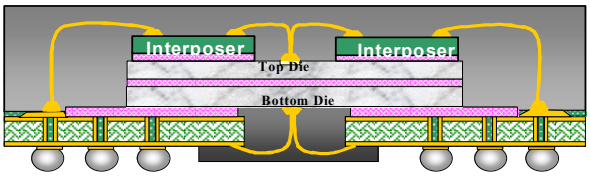


Fig. 2. D2i-wCSP Structure with Interposers.

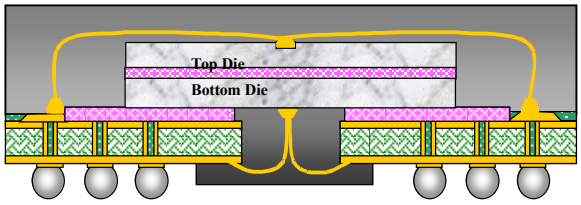


Fig. 3. D2-wCSP Structure without Interposers.

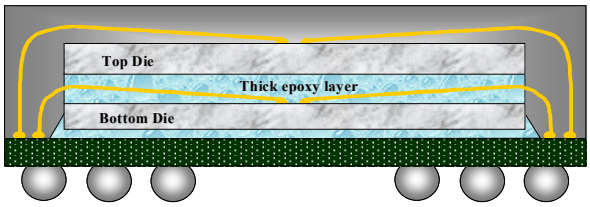


Fig. 4. D2-FBGA Structure with both Dice Facing Package Top.

The D2(i)-wCSP structure presents a suitable packaging option for memory devices with a single row of bond pads. With the increase of memory density and thus greater I/O connections requirement, package design would need to accommodate memory chip design with two rows of die bond pads. D2(i)-wCSP stacked die structure will be of less ideal for chip design with two rows of die bond pads. With the consideration of mirror effect, after wirebonding from the bond pads of the top die to the substrate, extra traces have to be routed from one end to the other of the substrate in order to establish connection with their respective matched pins at the bottom die. This cross routing of traces will make the substrate design more complicated and extremely difficult for high I/O counts. Therefore for a high I/O memory device with two rows of die bond pads, a need exists for innovative stacked structure that allows the top and bottom dies to align in a common direction within the package.

Fig. 4 shows a package structure for D2-FBGA. This package design allows the active faces of the two stacked dice to align upwards. In this manner, no cross routing of

traces for the top die pins is needed for connection with the matched pins at the bottom die. And the window opening on the substrate can be eliminated, thus allowing more space for trace routing flexibility.

Although D2-FBGA can resolve the drawback of substrate design on D2i/D2-wCSP, good electrical performance is critical for package solution selection. In general, low parasitics of resistance (R), inductance (L) and capacitance (C) are desired. However due to the inclusion of additional die for increased memory capacity in a single package, simultaneous achievement of both net length matching between the top/bottom dice and low capacitance has to be compromised. For instance in D2-FBGA design, low capacitance is achievable in the expense of high inductance in some signal pins (although with matching net length). As for the D2i-wCSP version, lower inductance can be achieved for the bottom die but with non-matching net length with the top die and a higher capacitance. Another version of stacked die wCSP is developed, namely 2DD2-wCSP as shown in Fig. 5. This package contains two stacked dice with the active faces in line with the package bottom. Compared with D2-FBGA, all the long bonding wires are replaced by metal traces inside the substrate thus resulting in a lower inductance. It also provides a better net length matching between top/bottom dice with a lower capacitance when compared to the D2i-wCSP package.

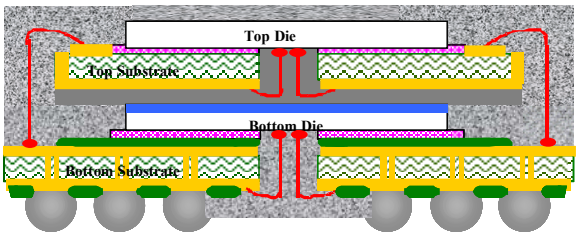


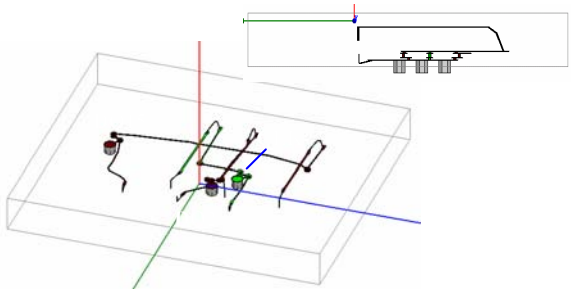
Fig. 5. 2DD2-wCSP Structure with both Dice Facing Package Bottom Direction.

2. Electrical Performance Consideration

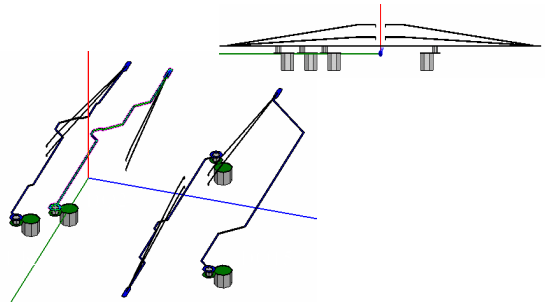
Good electrical performance is a key driving factor for selecting a suitable package design. Low electrical parasitics in resistance (R), inductance (L) and capacitance (C) of an IC package are desired. In the current proposed stacked die memory packages, it is important to understand the electrical characteristics of each package type in meeting different customers' requirements and applications. A 3-dimensional (3D) electrical simulation was performed using Ansoft Q3D, with the package parasitics of RLC compared in Table 1. The packages modeled were D2i-wCSP, D2-FBGA and 2DD2-wCSP, with a common package size of 11.4x12.5mm and a die size of 9.32x9.49mm (dual center bonding pads). Three nets of "CLK", "DQ2" and "DQ15" were selected for analysis, with each net consisted of connection from the top/bottom dice and routed according to the respective package design. The solder ball pin assignment is assumed to be the same for all three packages. The respective 3D simulation models are shown in Fig. 6.

Table 1. Comparison of RLC for Different Package Types.

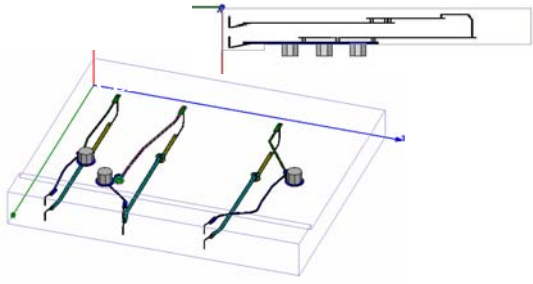
Pk Type	Net	R (mOhm)		L (nH)		C (pF)
		Top	Bot	Top	Bot	N.A.
D2i-wCSP	CLK	270	80	7.91	2.39	0.58
	DQ2	260	60	7.02	1.57	0.54
	DQ15	390	120	15.6	3.84	0.61
D2-FBGA	CLK	440	420	8.61	7.39	0.14
	DQ2	400	390	9.11	8.81	0.15
	DQ15	440	430	12.45	12.3	0.17
2DD2-wCSP	CLK	200	76	6.21	2.28	0.28
	DQ2	221	56	6.78	1.49	0.32
	DQ15	183	103	6.84	3.71	0.28



i) D2i-wCSP



ii) D2-FBGA



iii) 2DD2-wCSP

Fig. 6. 3D Models for i) D2i-wCSP, ii) D2-FBGA, iii) 2DD2-wCSP.

In the D2i-wCSP design, a similar die is being flipped over and stacked onto the bottom die. As explained in the preceding section due to the result of mirror effect, the pairing pin of the top die (for instance "DQ15") has to be routed from one end to the other end of the substrate for the connection with its matched pin on the bottom die. Long connecting trace has to be routed on the substrate thus

resulting in a high inductance (L = 15.6nH). Although low inductance can be achieved for the bottom die, the resulting mismatch in the inductance of the pairing pin may affect its electrical performance and integrity of the signal.

With the D2-FBGA design where both dice are facing upwards, the direct wire bonding method will provide a much better match in the trace length of the pairing pin thus solving the mismatch issue in inductance. It can also be seen that the capacitance of the three nets is the lowest among the three package types. The only concern lies with the higher inductance contribution. In the top die where a longer bond wire is needed, the inductance will be higher than a net that is formed by copper trace (per D2i-wCSP design, "CLK" and "DQ2" nets). With the additional need of routing from one to the other side of the substrate due to commodity pin assignment conformation, the extra trace length gave rise to an increase in the inductance (significant increase in the bottom die). Nonetheless in the case where the inductance values meet customer specifications, the matching inductance will provide an optimal electrical performance.

The 2DD2-wCSP can be viewed as an accommodating design where an improvement of the capacitance can be achieved over the D2i-wCSP design, at the same time providing better inductance matching. Using "DQ15" net as an illustration where the two stacked dice are facing down, the routing of the long trace for the top die is being eliminated thus resulting in a lower inductance (L decreases from 15.6nH to 6.84nH). When compared with D2-FBGA, the long bonding wires are replaced by metal traces inside the substrate for the 2DD2-wCSP package. Hence inductance decreases as a result ($L_{wire} > L_{copper\ trace}$). From the above observations, the 2DD2-wCSP design offers a good package solution for concurrent electrical requirements of low inductance, low capacitance, and closely matched net lengths. The above investigation revealed the different electrical characteristics of the three package types. Hence careful selection of a package solution is necessary in meeting customer specific electrical requirements.

3. Board Level Reliability Consideration

Package assemblies are exposed to a wide range of external loadings both in the phase of production as well as during field usage. For BGA packages, solder joints provide both the electrical and mechanical connections between the device and the printed wiring board (PWB) module. Thus, damage to solder may readily affect a system's functional integrity. Solder fatigue reliability during temperature cycling (T/C) is an important qualification requirement which determines the suitability of the package for on-board application [2-4]. To date, actual accelerated T/C testing had been conducted on D2-wCSP while testing for the other package types are under development. Upfront analyses using the Finite Element Method were also performed in consideration of package optimization at the design stage prior to the implentation of actual T/C test, which can be time consuming and hitting on the time line of product development.

In the current test vehicle for D2-wCSP, a sample size of 32 units were included in the test matrix to provide adequate determination of the weibull slope and the characteristic life. The package was daisy chained to the die with full joints monitoring on the board side. Shown in Fig. 7 is the specification of the package build. The solder joints were of 63Sn/36Pb/2Ag composition with a ball diameter of 0.45mm prior to reflow. The packages were surface mounted onto a PWB, which can accommodate 12 units (with individual isolation slots) per panel. The package integrity was assessed prior to the temperature cycling test with a range of –40 °C to 125°C, with ramp and dwell loads at 15 minutes interval each at approximately 1 cycle per hour.

Package Type	D2-wCSP 90B; Size: 13.0x8.0mm
Die Quantity	2 similar dies
Die Size	5.0x 9.7mm
Substrate	UTAC design - daisy chain to die

Fig. 7. Specification of D2-wCSP for T/C Test.

Based on the current test-setup, D2-wCSP achieved a T/C characteristic life of 1697 cycles as shown in the Weibull plot of Fig. 8. All failures had been verified to be solder failure due to ball joint cracking (see Fig. 9). Prior to actual testing, a numerical model based on the exact package setup was analyzed. Shown in Fig. 10 is a quarter model of the D2-wCSP. Darveaux's methodology [5] was implemented for the current analysis. Numerical prediction showed a T/C life of 1,468 cycles, achieving an accuracy of within 13% compared to the actual T/C result. Similar methodology with the same material set was extended to the analyses for 2DD2-wCSP and D2-FBGA. Fig. 11 shows the half 2D view of the respective models. 2DD2-wCSP showed a higher reliability (close to 10% increase) compared to D2-FBGA and D2wCSP, which were observed to yield comparable performance in terms of board level T/C reliability. This trend provides upfront comparison for the 3 different package designs, in aid of better design focus during the development stage. Actual performance remains to be validated.

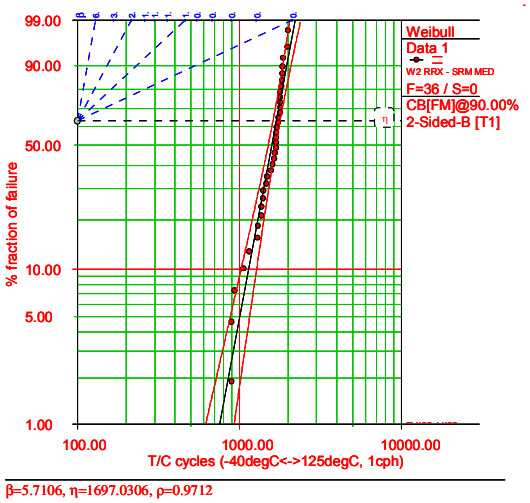


Fig. 8. Weibull Distribution for D2-wCSP.

Fig. 9. Optical Micrograph Showing Solder Crack.

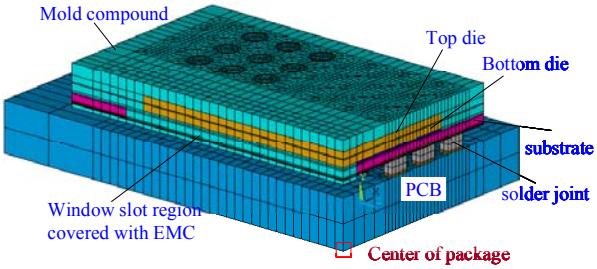


Fig. 10. Quarter Model for D2-wCSP.

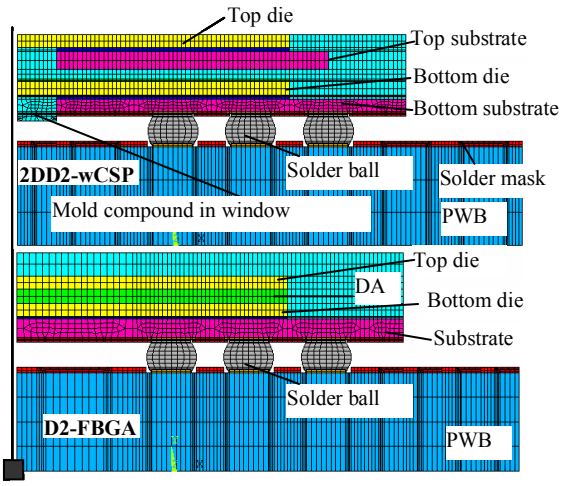


Fig. 11. Half 2D View of 2DD2-wCSP and D2-FBGA.

4. Package Assembly Processes

4.1. D2i/D2-wCSP

The manufacturing process of D2i-wCSP is similar to the D2-wCSP except with the inclusion of interposers which acts as the bridge for long wire connection. The assembly process flow is shown in Fig. 12. Due to the presence of interposers, D2i-wCSP will have a higher material and process cost compared to D2-wCSP. Also, under the same package height constraint, D2-wCSP can accommodate a thicker die thickness thus presenting a lower process risk and costing due to lesser wafer backgrinding and wafer mount process steps. However, D2-wCSP requires tight wire looping control for wire bonding on the top die as the long wires need to traverse a larger part of the die surface from die center. Long wire poses a challenge to the molding process also in terms of wire sweeping control. Fig. 13 shows the SEM images for D2(i)-wCSP prior to the molding process.

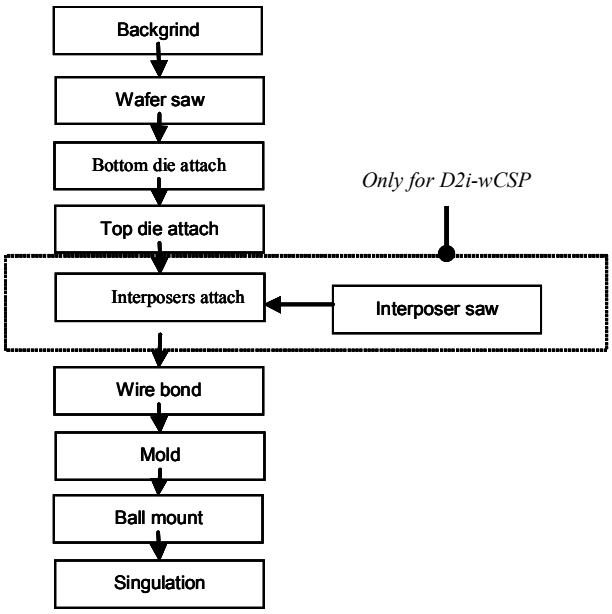


Fig. 12. Assembly Process Flow for D2i/D2-wCSP.

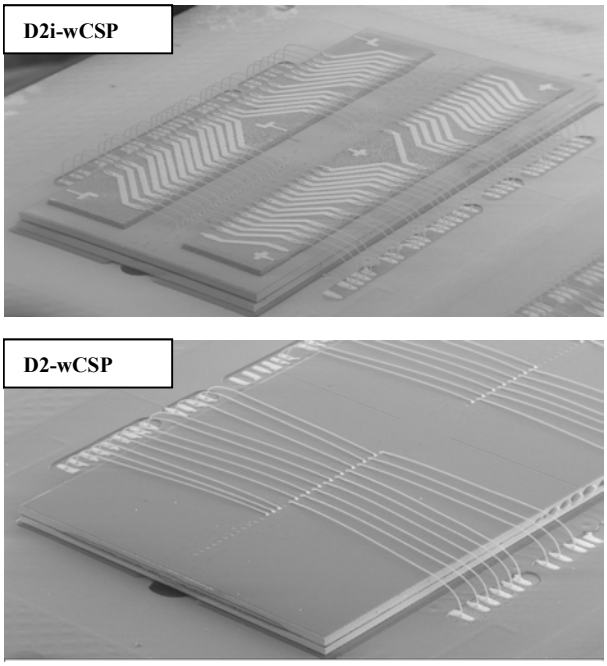


Fig. 13. SEM Photos for D2i/D2-wCSP.

4.2. D2-FBGA

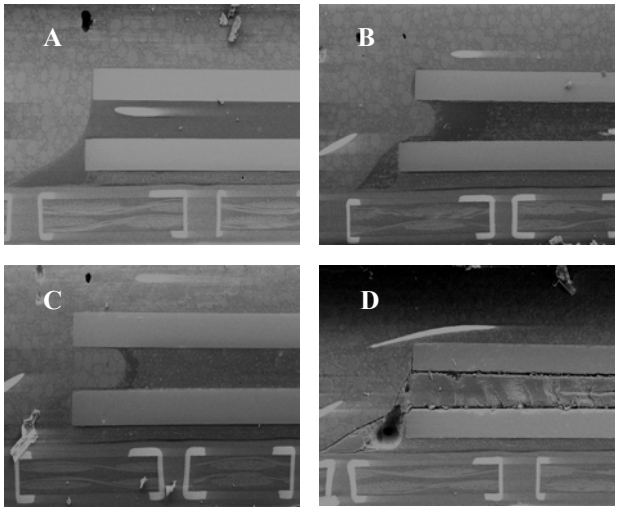
The manufacturing process flow of D2-FBGA is similar to conventional stacked die packages. However, there are several main challenges faced in the D2-FBGA process and they are briefly described below:

Selection of Die Attach Epoxy Between Top/Bottom Dies

As the long bonded wires need to go through two types of epoxy materials namely die attach (DA) epoxy and mold

compound, it becomes critical to evaluate the top DA epoxy with the requirements as follow:
- Low shrinkage after cure. As high shrinkage of epoxy will cause additional stress to bonded wires, resulting in potential lifted or broken wire.
- To reduce the mismatch of CTE with mold compound. Delamination may occur due to mismatch of CTE between DA epoxy and mold compound, resulting in potential bond wire tearing during thermal cycling test.

Fig. 14 illustrates some scenarios of DA epoxy with various degrees of shrinkage and the separation resulted by material shrinkage and CTE mismatch with other package materials.



a) Epoxy A has no shrinkage after cure.
b) Epoxy B has a slight shrinkage after cure.
c) Epoxy C has serious shrinkage after cure.
d) Epoxy D has high CTE mismatch with mold compound, and delaminiation occurred at the interfaces.

Fig. 14. DA Epoxy Shrinkage After Cure and CTE Mismatch with Mold Compound (D2-FBGA).

Bond Line Thickness (BLT) Control for DA Epoxy Between Top and Bottom Dies

Compared with BLT of conventional die attach process which is around 1mil (25um), a much thicker epoxy layer is required for die attach between top and bottom dies for D2-FBGA to accommodate sufficient space for wire bonding loop on the bottom die. Based on internal process evaluation, a 160um BLT is needed for 4.5 to 5mm long wires on the bottom die.

Wire-sweep Control for Bonded Wires on Top Die During Molding Process

In order to reduce wire sweep for bonded wires on the top die, several factors need to be considered. It is essential for mold gate design to allow mold compound flow in the direction of the wire span, as well as the optimization of molding process parameters. Additional interposers can be incorporated on the top die surface which helps to promote shorter wire length as in D2i-wCSP.

4.3. 2DD2-wCSP

2DD2-wCSP involves the most complicated stacking assembly process using the package-in-package concept. Fig. 15 details the assembly process flow:

1. Top die is attached on top substrate and wire bonded.
2. Top die portion is molded and singulated to be a package.
3. Bottom die is attached on bottom substrate and wire bonded.
4. Top package is attached on bottom die, and following the same direction as bottom die – facing package bottom surface.
5. Finally mold the whole package.

Fig. 16 shows the SEM photo of the 2DD2-wCSP structure.

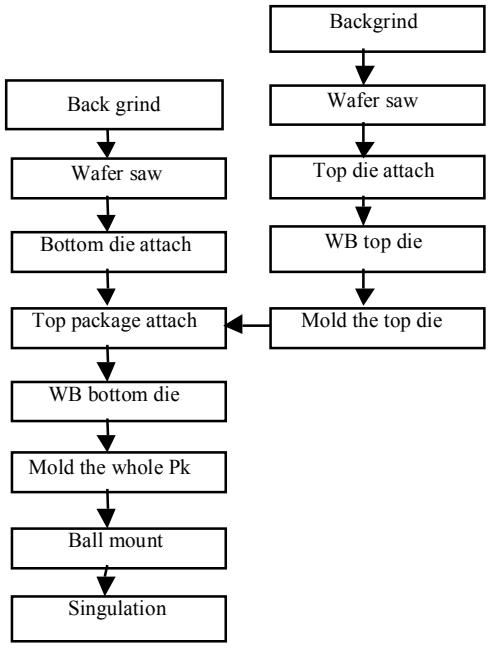


Fig. 15. Assembly Process Flow for 2DD2-wCSP.

Fig. 16. SEM Photo for 2DD2-wCSP.

5. Package Level Reliability Tests

All the above mentioned stacked die packages of D2(i)-wCSP, D2-FBGA and 2DD2-wCSP went through internal package level reliability tests, with all passing the tests. Below are the conditions and criteria of the reliability tests:

1) MSL3: 30°C/60%RH, 192 hours, 3xIR reflow with 260°C. Sample size = 135 units.
2) Temperature Cycling: -65°C/150°C with 1000 cycles, 2 cycle/hour. Sample size = 45 units.
3) High Temperature Storage: 150°C with 1000 hours. Sample size = 45 units.
4) Autoclave: 120°C/100%RH/2atm with 168 hours. Sample size = 45 units.

6. Conclusions

This paper presents the different options for a stacked die memory package, with the various aspects of design, electrical performance, assembly processes, board level solder joint reliability and package reliability being addressed. The work outlined the challenges in the assembly process, the comparison of the packages' electrical characteristics and solder joint fatigue lives under thermal cycling test. Recommendation for suitable package solution will be dependent on customers' requirements and applications, along with others considerations such as ease in assembly, materials availability and selection, cost and package performance.

Acknowledgments

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