On the Thermal Characterization of an Exposed Top Quad Flat No-Lead Package

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Abstract

The relentless trend of ever increasing integrated circuit chip functionality and decreasing chip dimensions for miniaturization of products have led to intense heat dissipation in IC chips. The problem of effective cooling of chips at an acceptable cost is now becoming an urgent issue[1]. Leadframe CSP package is a promising candidate for portable wireless applications such as Bluetooth and home RF. It offers attractive attributes in terms of a near CSP footprint, good electrical and thermal characteristics. This paper addresses the concern and possible solution when conducting thermal characterization of an Exposed Top Quad Flat No-Lead (et-QFN) package, which had successfully been developed and qualified in United Test and Assembly Center (UTAC). Studies were performed to assess the impact of JEDEC test board types, with/without metal housing under different air speeds using commercial CFD code and the same is validated with experiment results. FA tools were used to pinpoint factors that are to blame for the significant measurement errors observed. Good agreement could be achieved between simulation and testing results when these factors were included into the CFD models. Recommendations regarding SMT and modification of specifications of 2s2p JESD51 PCB are proposed and discussed.

Keywords: et-QFN, thermal resistance, CFD modeling and simulation, thermal measurement and validation

1. Introduction

Quad Flat No-Lead (QFN) is a leadframe-based package, which offers thermal and electrical enhancement with its exposed die pad on the bottom of the package surface. The exposed die pad not only provides an efficient heat path to the package top, but also enables stable grounding with electrical connection through a conductive die attach material. QFN is a cost effective option for small packages with low to medium lead count. It is an ideal choice for telecommunication products like cellular phones and wireless LANs, portable consumer products such as PDA and digital camera, and automotive electronics system.

For standard QFN, it is well known that best thermal performance can be achieved by directly attaching the die pad to PCB Cu land, under which there are array of thermal vias connecting ground plane[2,3,4]. However, due to the continuing drive of functional integration and system miniaturization, heat and trace density on chip and board keeps increasing. In some cases, the PCB mounts so many components that it becomes thermally saturated. On the other hand, the high wiring density makes it impossible for the PCB to afford a thermal attachment area or any thermal vias. Moreover, some applications involve only low conductive PCB, e.g. 1s1p or flex. Heat generated by devices is extremely difficult to dissipate through the PCB. To address these concerns, UTAC has successfully developed a low profile package called et-QFN, which is able to dissipate heat from the top of the package.

2. Construction of et-QFN

Fig. 1 illustrates the design of an et-QFN. It takes advantage of both half etching and leadframe up-setting know-how to expose the paddle on the top of the package side with a die down assembly configuration.

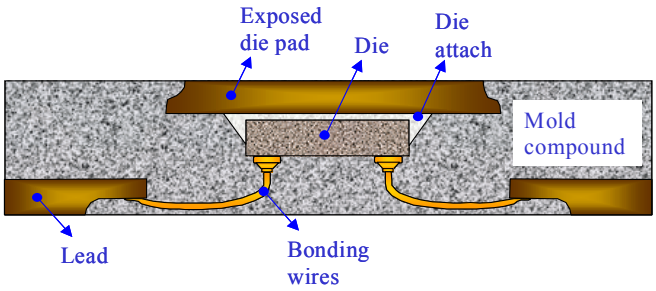

Fig. 1 et-QFN structure

Main drawback of this package compared with standard QFN package includes:

1. Needs to reconfigure the pin assignment during design stage
2. 2-tier wire bonding is not possible due to the construction feature of the half etch leads which constraint the height of the wire loop
3. Incurs additional up-setting tooling cost

Nevertheless, it is a very reliable package, which offers an ideal packaging solution for small device and with metal housing, is able to handle high power by dissipating it through package top, minimizing thermal cross talk with its surrounding components.

3. Description of test vehicle and procedure

In order to evaluate the package thermal performance, a 32 lead et-QFN 5x6mm was selected as test vehicle. Temp01 thermal test die[5] was used for this package since the die paddle can only accommodate a very small die. The thermal test die contains temperature sensing diodes and heating resistors. They were connected from the die to the leads of the package through bonding wires. Note that not all the leads

were wire bonded and used in thermal measurements. Package details are summarized in Table 1

.

Table 1 Package details

Die Size	1.3716 x 1.397 mm
Total no of wires	8
Wire Diameter	24.5mm
Lead-frame Material	C194
Lead-frame Thickness	0.2mm
Paddle Size	2.8 x 3.8mm
Package Size	5 x 6 x 0.9 mm

The finished samples were manually mounted on a thermal test PCB as per JEDEC specification JESD51-3[6] and JESD51-7[7] as shown in Fig 2.

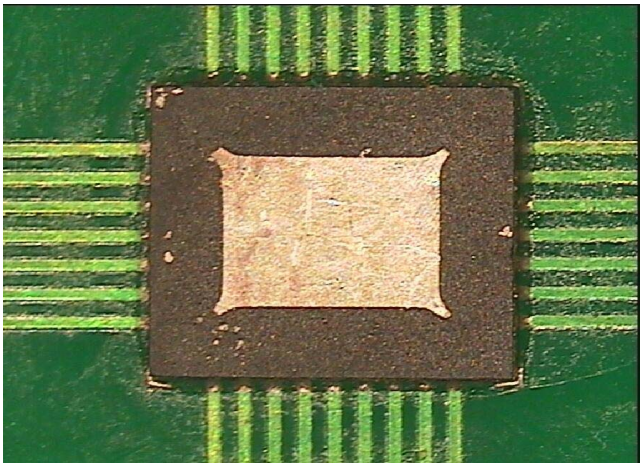

Fig. 2 et-QFN soldered to thermal board

A nickel-plated copper heat spreader of 40x40x0.5mm in size was selected to represent metal housing in actual application since its size is not available. Evaluation was conducted according to the matrix defined by Table 2. A thermal test sample size of 5 was used for each testing configuration and the result was averaged and compared with prediction made by CFD simulation.

Table 2 Characterization matrix

Test conditions with 0, 1 and 2 m/s wind speed		
PCB	Metal housing	
	Without	With
1s0p	x	x
1s2p	x	x

As per JEDEC JESD 51-1[8,9], junction temperature was measured by standard Electrical Test Method. Before actual measurement was carried out, each thermal test die was subjected to standard K factor calibration against Memmert ULP 400, a precision programmable heating oven. At first attempt, the diode bridge was used but it was too sensitive to the change of environment. As a result, all calibration and measurement were performed using single diode.

For free or forced convection thermal performance evaluations, the test board was mounted at the center in a

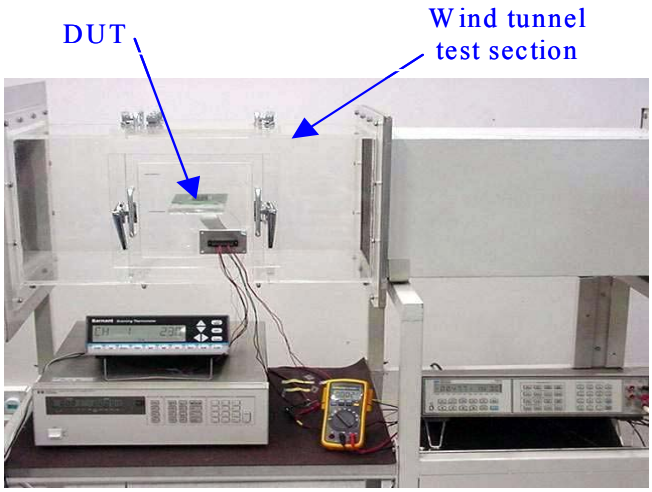

Fig 3. Force convection measurement setup

JEDEC standard still air test chamber or wind tunnel[10,11]. Fig. 3 depicts the forced convection test setup. To improve the signal to noise ratio, 0.5W power was supplied to the thermal die for the package without metal housing while 1W was delivered to the package with metal housing.

4. CFD modeling

FLOTHERM®[12], a leading Computational Fluid Dynamics (CFD) software code specially developed for the electronics industry, was employed to predict the package thermal performance for each test condition. Fig. 4 depicts the solid model of et-QFN.

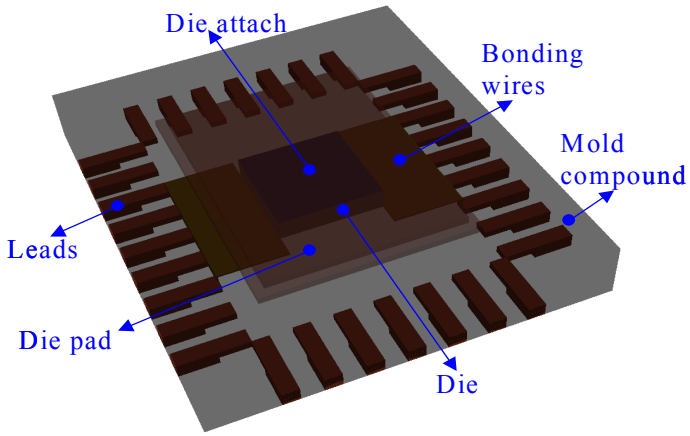

Fig.4 Flotherm solid model

Some intricate shapes might not be necessary to model it in CFD tool. Moreover, the CFD model sholud represent the exact physical structure. For all the cases studied package parts were represented as a series of embedded conductive solid cuboidal blocks with either isotropic or orthotropic thermal conductivities. Radiation was applied to all the

exposed surfaces, whose emissivity was assumed to be 0.8. Material properties are listed in the table 3.

Table 3. Material Properties

S/n	Material	K (W/mK)
1	Mold Compound	0.96
2	Die Attach	0.6
3	Leadframe	260
4	Heat Spreader	262
5	HS attach	1.5
6	PCB dielectric	0.3
7	PCB trace	390
8	Solder	50.9
9	Die	Temp. dependent*
10	Bond wire	296

*K(Si)=117.5-0.42 (T-100)

Localized grid was used to capture temperature profile and flow pattern in the areas of interest or where rapid changes are expected. Grid-dependent solution studies were performed by adjusting grid size. It is assumed that a converged result has been achieved if the junction temperature is changed by less than 1% with a finer gridding.

Laminar and turbulent flow were assumed for natural and forced convection respectively with ambient temperature of 25°C. Fig. 5 shows the temperature profile for et-QFN without metal housing on a 1s0p test board under natural convection.

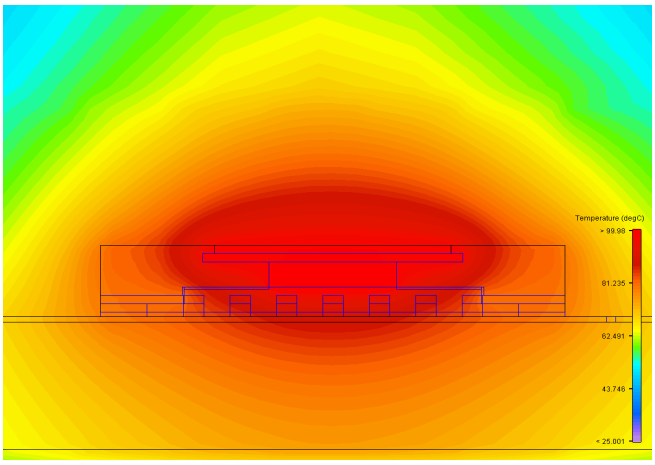

Fig. 5 Cross-sectional temperature plot

5. Results and discussion

The mean thermal performances were found in the experiemental results of 5 samples of each test. Thermal behaviors/performances are shown in Fig. 6 and Fig. 7 for the 32L et-QFN 5x6mm on JEDEC 1s0p and 1s2p standard test board respectively at 0, 1, and 2m/s airflow speed. They are plotted against the simulated (predicted) results on the same graph. It is found from the graph that 70% (maximum) thermal performance improvements can be achived when a metal housing is attached to the package top.

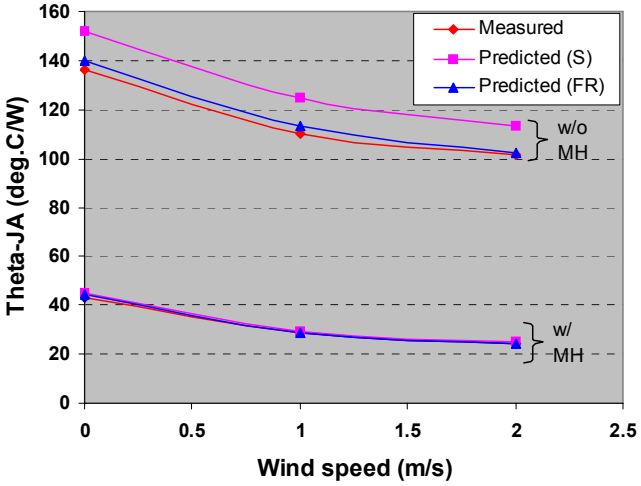

Fig. 6 Measured and predicted thermal performance of et-QFN on a 1s0p JEDEC test board

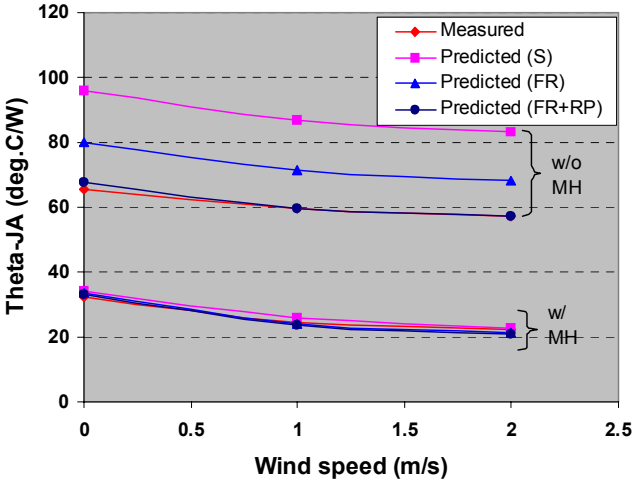

Fig. 7 Measured and predicted thermal performance of et-QFN on a 1s2p JEDEC test board

Under standard (S) or perfect simulation condition, the following observations can be made,

1. When a Metal Housing (MH) is attached to the package top, the measured thermal resistances are quite close to what have been predicted by simulation, whether the package is mounted on a 1s0p or 1s2p thermal test board. However,
2. When there is no metal housing attached to the package top, the measured thermal resistances are far away from those predicted values. It is always true no matter what test board type is used.
3. The extent of deviation is different. A much larger error is found for packages soldered to a 1s2p PCB than those soldered to a 1s0p PCB.

It was found from the simulation that the major heat flow path (70~90%) is from package top to ambient air if a metal housing is used. In this case, the measurement results agree well with the simulated ones. However, if most of the heat generated on die flows through package bottom to PCB and to

ambient eventually, i.e. when there is no metal housing attached to package top, huge errors were observed. It was realized that board assembly process such as application of flux and PCB layer stack up thickness and its distances might have induced the errors in the measurements.

Using optical microscope, failure analysis were carried out to inspect the surface mount quality. Fig. 8 provides the cross-section of the test sample, a zoom-in view shows that the flux residue has occupied the gap between package and PCB even though air gun was used to clear the flux since the package was assembled onto the PCB manually. The flux helps to reduce the thermal resistance and hence enhance package thermal performance. Therefore, if the PCB is not saturated and the routing difficulty is the only reason to justify et-QFN application, then one may intentionally use non-clean flux for board assembly to further reduce junction temperature.

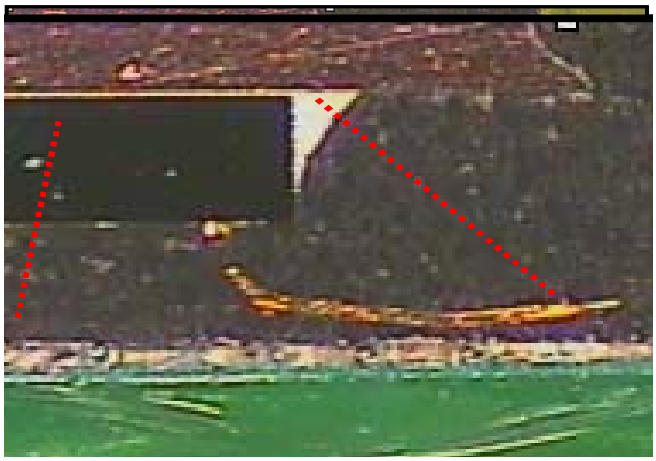

Fig.8 Cross-section of et-QFN

The CFD model was then modified to reflect the change of air gap to flux residue (FR), the results was updated accordingly. It can bee seen from Fig. 6 that the maximum difference between the measured and predicted theta JA values is less than 5% for test samples with 1s0p PCB. However, for packages with 1s2p PCB as shown in Fig. 7 the experiment results are still very far away from the newly predicted ones. It is quite natural to look into the PCB quality for possible causes. Failure analysis was conducted using SEM. Fig. 9 displays the cross-section image of a 1s2p test board.

It is found clearly that the thickness of core and prepreg is 1.0mm and 0.25mm respectively. Although it is still compliant with JEDEC/JESD51-7 standard (Fig. 10), it is evident that it is at the lower limit in terms of prepreg thickness.

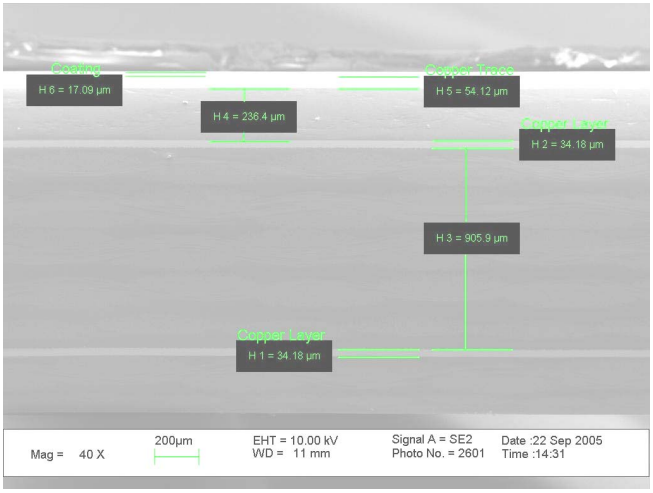

Fig. 9 SEM analysis of 2s2p test board

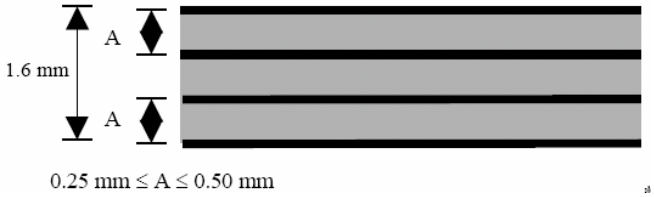

Fig. 10 JEDEC/JESD51-7 specifications

The CFD model was checked for PCB structure. It is found that the prepreg was modeled with 0.25mm thikness, the default value for 2s2p board model downloaded from Flopack[13]. It is at its upper limit of high conductivity PCB specification. When a reduced prepreg (RP) thickness is used, the measurement and simulation agreed within 8% or better (Fig.7). As the tested package is very small, the thinner prepreg of test board helps to spread the heat through inner copper planes and the junction temperature can thus be reduced. Therefore, for packages with small body size on a high conductivity test board, thermal performance is very sensitive to the prepreg thickness of the PCB. In such cases, it is suggested to measure the actual pregreg thickness and include it in the test and simulation report.

6. Conclusions

Three-dimensional CFD simulations were adopted to analyze thermal performance of a newly developed QFN. It was found that with a metal housing, the package is possible to achieve thermal improvement by about 70% compared to the package without metal housing at the top. In addition, up to 90% of the die power could be dissipated through the package top in this case. During measurement, however, significant discrepancy was observed as well, especially for those on a 2s2p test board. To identify the root causes, failure analysis was conducted using SEM and X-section. It was concluded that the flux residue and distance between the top signal layer and inner ground layer were responsible for the errors observed. If these two factors were taken into account, the

agreement between measurement and simulation result was within 8%. In view of their strong influence on thermal performance of packages with small body size, care must be taken to control of SMT process and supplied PCB must be measured and the actual data should be reflected in modeling and testing report.

Acknowledgments

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