Optimization of Flip Chip Interconnect Reliability Using a Variable Compliance Interconnect Design

Andrew A.O. Tay and Wei Sun*
Nano/Microsystems Integration Laboratory
Department of Mechanical Engineering
National University of Singapore
Email: mpetayao@nus.edu.sg

*Now with United Test and Assembly Center Ltd, Singapore

Abstract

This paper describes a finite element parametric study of the reliability of the solder joints of a flip chip package in which the height *H* and diameter *D* of copper column interconnects are varied. It was found that when *D* was kept constant at 50µm while *H* was varied, from 25µm to 150µm, there was a local optimum at around *H*=50µm. Thus while the compliance of the interconnect with *H*=100µm was greater, it did not lead to a longer fatigue life. However, beyond *H*=125µm, any increase in length/compliance did lead to a longer fatigue life. Similarly, when the interconnect height *H* was kept constant at 150µm while the diameter *D* was varied from 15µm to 35µm, it was found that a local optimum existed at around *D*=25µm. Next a simulation was conducted in which the height of the interconnects *H* was kept constant at 150µm while the diameter *D* on the same chip was decreased continuously from 35µm at the center to 15µm at the perimeter of the chip. It was found that this case where the compliance is low at the center and high at the perimeter of the chip gave fatigue lives which were more than double that of the local optimum case mentioned above where *D* was constant at 25µm. Hence, an interconnect design where the compliance of the interconnects on the same chip is varied from a low value at the center to a high value at the perimeter will lead to optimum reliability of the critical solder joint.

1. Introduction

Flip chip packages are required to survive at least 1000 cycles of temperature cycling. With cyclic changes in temperature, the stresses in the interconnections will vary in a cyclic fashion and lead to fatigue failure of the interconnects or solder joints, typically the latter. Generally speaking, the further the interconnection is away from the centre (neutral point) of the chip, the greater the stress induced due to the mismatch in CTE between chip and substrate. This interconnect is called the critical interconnect. In order to reduce the stresses induced in the solder joints, and hence improve the fatigue life of the joint, attempts have been made to increase the compliance of the interconnections. However, it has often not been realized that increasing the compliance of interconnects does not necessarily lead to improvements in the fatigue life of the critical joint, unless the compliance is beyond a threshold value. This is because all the interconnects play a part in accommodating the thermal mismatch between the chip and the substrate. If the interconnects are stiff, the displacements of the critical interconnect will be reduced. On the other hand, if the interconnects are compliant, the stress induced for the same displacement will be reduced.

Borgesen and Li [1] analysed the stresses in flip-chip solder joints of spherical (convex) and hourglass (concave) shapes. They employed an analytical approach and considered only elastic behaviour. They used the maximum tensile stress in the solder joint as an indicator of the reliability of the joint. The greater the tensile stresss in the joint, the lower the reliability (fatigue life). They showed that the maximum tensile stress in the critical interconnect is lower if the solder joints were all of the hourglass shape compared to the situation when the joints were all spherical. They further showed that if the solder joints in the central region were of the stiffer spherical shape and those near the perimeter of the package were of the hourglass shape, the best reliability can be achieved.

Kacker et al [3] compared the reliability of flip-chip packages employing three different arrangements of interconnects: (a) all interconnects of high-compliance G-Helix interconnects, (b) all interconnects of stiff column interconnects, and (c) a mixture of interconnects are used - stiff copper column interconnects in the central region of the package, high-compliance G-Helix interconnects at the perimeter and low-compliance G-Helix in the region in between. They found that the arrangement (a) gave the best reliability.

The case considered in this study is the optimization of copper column interconnects for a wafer level flip chip package. Improvement in reliability is explored in terms of varying the compliance of the interconnects by varying the diameter and height of the interconnects. Two-dimensional finite element simulations are carried out on the fatigue life of solder joints in a chip of length 8 mm and thickness 640 µm which is connected to a substrate of thickness 800µm by copper pin or column (CuC) interconnects. The package is subjected to temperature cycling between -40°C and 125°C. Both chip and substrate are modelled as temperature-independent linear elastic materials. Copper is assumed to be a temperature-independent elastic-plastic material while eutectic tin-lead solder is modelled as a temperature-dependent elastic-plastic material.

2. Parametric Study

A parametric analysis of the reliability of the solder joints will be carried out in which the diameter *D* and height *H* of the interconnect are varied in order to vary the compliance or stiffness of the interconnect. The stiffness of a structure is the

reciprocal of its compliance. The pitch of the interconnects is 100μm. It has been shown that for a parametric analysis, a two-dimensional finite element analysis is adequate [3,4] in determining the relative effects of various parameters on the fatigue life of the solder joints. The two-dimensional finite element model employed in the analysis is shown in Fig. 1.

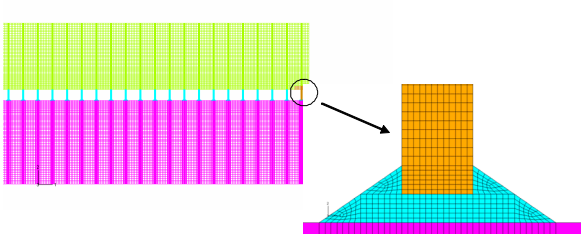


Fig. 1 Finite element model of interconnect, solder joint, chip and substrate.

Since copper is stronger than solder, failure usually occurs in the solder joint through fatigue. It has been shown that solder fatigue failure during temperature cycling can be predicted using the Incremental Equivalent Plastic Strain Range, $\Delta\varepsilon_{eq}$, experienced by the solder during a cycle [4]. In the numerical simulations performed, it was found that the stress-strain hysteresis loop converges at about the 5th cycle. Hence, the parameter used to determine the relative reliability or fatigue life of the solder joint is the $\Delta\varepsilon_{eq}$ between the 4th and 5th cycle. The following Coffin-Manson-type empirical correlation [4] will be used to predict the fatigue life N_f of the solder:

$$N_f = 0.4405(\Delta\varepsilon_{eq})^{-1.96} \qquad (1)$$

Typical distributions of the Equivalent Plastic Strain (EPS) obtained is shown in Figure 3. It is usually found that the finite element where the EPS of the solder is the maximum is also the element, called the critical element, where the range of variation of the EPS is the maximum. As can be seen from Figure 3, the EPS varies considerably over the solder joint. The maximum value is rather localized around the critical element. It is generally accepted that if the EPS of the critical element is used to estimate the fatigue life, the predicted magnitude of the fatigue life is likely to be underestimated. On the other hand, if the average over the entire volume of the solder joint is used, the predicted fatigue life is likely to be grossly overestimated. The optimum region over which to average the EPS in order to obtain an accurate prediction is likely to be a small group of elements around the critical element. The value of the incremental equivalent plastic strain range obtained by averaging over a certain volume of the solder is called the Volume-Weighted Incremental Equivalent Plastic Strain Range (VWIEPSR). This value is taken to be the $\Delta\varepsilon_{eq}$ to be used in equation (1) to estimate the fatigue life of the solder joint.

Three different regions will be used to calculate the VWIEPSR and analyze the effect of the interconnect height on the reliability of the solder joints. The three methods are illustrated in Figure 3. In Method 1, called Local, the region considered is the critical element at the corner where the maximum plastic strain range occurs and the 3 elements around it as shown in Figure 3(a). In Method 2, called Two-Layer, the region considered is the 2 layers of altogether 10 elements around the critical element as shown in Figure 3(b). In Method 3, called Corner, the region considered is the triangular region around the critical element as shown in Figure 3(c).

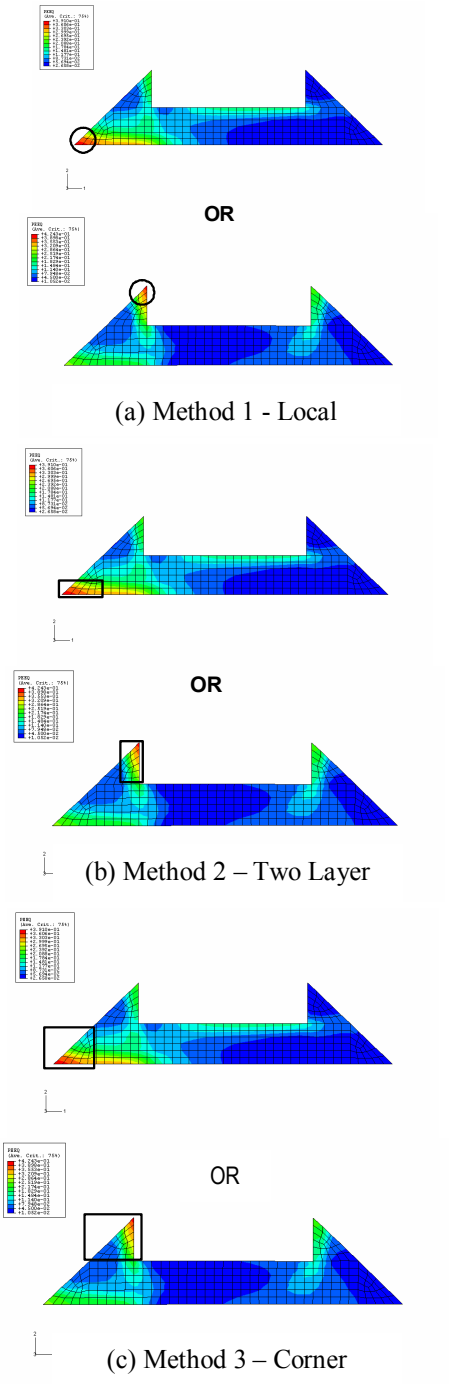


Fig. 3 Typical distribution of EPS in solder joint.

For the first series of simulations, the diameter of the CuC is kept constant at D=50μm while the height of the CuC H is varied from 25μm to 150μm. Values of $\Delta\varepsilon_{eq}$ obtained and the corresponding fatigue life of the critical solder joint are given in Table 1. As can be seen, for all the 3 methods used to calculate $\Delta\varepsilon_{eq}$, there is a local optimum height (compliance) of about 50 μm. For very tall interconnects, in this case beyond 125μm, it is true that the taller ie the more compliant the interconnect the longer the fatigue life of the solder joint.

Table 1 Variation of $\Delta\varepsilon_{eq}$ and fatigue life N_f with H.

	Method 1		Method 2		Method 3	
H (μm)	$\Delta\varepsilon_{eq}$	N_f	$\Delta\varepsilon_{eq}$	N_f	$\Delta\varepsilon_{eq}$	N_f
25	0.0612	105	0.0746	71	0.0429	211
50	0.0522	144	0.0462	182	0.0311	396
100	0.0560	125	0.0486	165	0.0320	375
125	0.0521	144	0.0445	196	0.0294	443
150	0.0470	176	0.0397	246	0.0263	551

The above finding may appear to contradict conventional wisdom that a greater compliance of the interconnect will *always* lead to a longer fatigue life. However, on closer analysis, this local optimum in interconnect compliance is reasonable. This is because all the interconnections contribute to accommodate the mismatch in the coefficient of thermal expansion (CTE) between the chip and substrate. For the case considered here, even though the 50μm high interconnects are stiffer than the 100μm ones, the stiffer interconnects in the central region of the chip can accommodate a greater portion of the CTE mismatch so that the critical interconnect at the perimeter of the chip has a lower strain and hence greater fatigue life.

This finding then leads to the idea that some further optimization may be achieved if the interconnects nearer the center of the package are made stiffer than those towards the perimeter of the chip. Then it might be possible for the stiffer interconnects in the central region of the chip to bear more of the CTE mismatch leaving the critical interconnect with a lower level of strain and hence achieving a higher fatigue life. This is the subject of investigations in the next section.

3. Variable Compliance Interconnect Design

In current practice, whenever it is desired to increase the compliance of the interconnects, the compliance of all the interconnects are usually increased equally. In other words, all the interconnects and hence their compliance, are kept identical. However, it will be demonstrated in this section that by allowing the compliance of the interconnect to vary along the chip, the reliability of the package can be enhanced. The package considered here is the same as that described in the previous section except that the interconnect height and the pad diameter are kept constant at 150μm and 50μm, respectively but the interconnect diameter is either kept constant or varied along the package. Since there is symmetry about the center of the chip, only half the chip is modeled. As the length of the chip is 8 mm and the interconnect pitch 100μm, there would be altogether 40 interconnects for half the chip length. Five cases are simulated as shown in Table 2.

Table 2 Case studies 1 to 5.

Case No.	Variation of interconnect diameter (D) from center to perimeter of package
1	D = 35μm throughout.
2	D = 25μm throughout.
3	D = 15μm throughout.
4	D varies from 35μm at center to 15μm at the perimeter (Big to Small).
5	D varies from 15μm at center to 35μm at the perimeter (Small to Big).

When the diameter of the interconnect is to be varied one can vary it continuously, for example from 35μm at the center of the package to 15μm at the perimeter. However, this will mean that the finite element mesh for each interconnect will have to be meshed individually which though not impossible would be very tedious. Hence, to reduce the computational effort, for Case 4, we will divide the 40 interconnects into groups of 8 with the same diameter. Case 4 is schematically illustrated in Fig. 4 where each interconnect pictured actually represents a group of 8 interconnects with the same diameter. In other words, the first 8 interconnects from the center of the package all have a diameter of 35μm. The next 8 interconnects all have a diameter of 30μm and so on until the last set of 8 interconnects all have a diameter of 15μm. However, it should be emphasized that it is not difficult in practice to fabricate interconnects of continuously varying diameters as the mask required can be easily produced using optical means with the aid of computer graphics. With this arrangement illustrated in Fig. 4, we have achieved a variation of the interconnect compliance with the least compliant in the center and the most compliant towards the perimeter of the package.

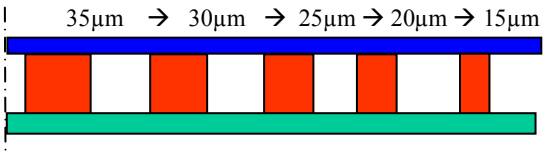


Fig. 4 Interconnect diameters for Case 4.

For Case 5, the diameter of the interconnects is also varied in groups of 8 except that this time the smallest diameter is placed nearest the center of the package. The purpose of this is to confirm which variation is more effective in maximizing the fatigue life of the solder joints.

The $\Delta\varepsilon_{eq}$ and the fatigue life N_f obtained using Methods 1 and 2 are shown in Table 3. Firstly comparing Cases 1-3, it can be seen that when the interconnect height is kept constant at 150μm in this particular study, there is an optimum interconnect diameter of about 25μm when the fatigue life is maximum at 288 cycles. However, from the results for Case 4, it can be seen that this fatigue life can be further increased to 633 cycles if we allow the compliance to vary along the package with the lowest compliance at the center and the

highest at the perimeter. Comparing Case 5 with Case 4, it is clear that having the bigger diameter at the perimeter does not help, possibly because the size of the solder joint is effectively smaller as the pad diameter is kept constant.

To provide further understanding of how the variation of compliance near the perimeter of the package might influence the reliability of the critical solder joint there, one further case is investigated. Case 6 is identical to Case 4 except that the diameter of the last set of 8 interconnects near the perimeter is increased to 20µm. As can be seen from Table 3, increasing the diameter of the interconnect in the last set near the perimeter of the package seems to lead to lower reliability of the critical solder joint.

Table 3 Fatigue life of solder joints for Cases 1 to 9

Case	Cryptic Description	Method 1		Method 2	
		$\Delta\varepsilon_{eq}$	N_f	$\Delta\varepsilon_{eq}$	N_f
1	All 35µm	0.0486	165	0.0408	233
2	All 25µm	0.0445	196	0.0366	288
3	All 15µm	0.0471	176	0.0402	240
4	Big to Small	0.0304	414	0.0245	633
5	Small to Big	0.0520	145	0.0440	201
6	Last Set 20µm	0.0490	163	0.0377	272
7	Variable Pad Size	0.0218	795	0.0160	1458
8	Variable Pitch	0.0192	1020	0.0140	1895

Variable Compliance with Variable Pad Diameter

It has thus far been established that a variable compliance interconnection design where the compliance of the interconnect increases with distance from the centre of the package leads to a higher fatigue life of the critical solder joint and hence higher package reliability. Apart from the beneficial effect of the variable compliance of the interconnect, another reason for the increased reliability could be the relatively large size of the solder joint at the critical interconnect. This is because the substrate pad size have been kept constant at 50µm even though the diameter of the interconnects towards the perimeter of the package have been reduced. In this section, the effect of substrate pad size is investigated. For Case 4, since the diameter of the interconnects are smaller towards the perimeter of the package, we could use smaller pads. This would also facilitate the fanning out of the metallization lines connecting the interconnects to other devices, as there will be more room between the pads for this purpose. The interconnection design with variable pad diameters is illustrated in Fig. 5.

As can be seen from Table 3, the fatigue life of the critical interconnection for this case is much better than Case 4. Thus even though the solder joint size for the critical interconnect is reduced, the fatigue life is significantly improved.

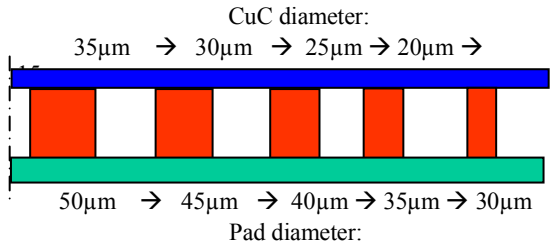


Fig. 5 Interconnect and pad dimensions for Case 7.

Variable Compliance with Variable Pitch

With the variable compliance and variable pad-size interconnect design represented by Case 7, the diameter of the interconnects and pads further away from the center of the package will be smaller. This affords the opportunity to decrease the pitch of the interconnects as their distance from the center of the package increases. This may be desirable in order to increase the total I/O of the package although one has to trade this off with the facility of fanning out metallization lines. The greater density of interconnects should improve the fatigue life of the critical interconnection. To illustrate this, a simulation is performed for a package where the interconnect diameter varies in groups of 8 in the same manner as in Case 4, with the interconnect pitch and pad diameter kept at 100µm and 50µm, respectively for all groups except for the last group near the perimeter where the pitch is reduced to 50µm and the pad size correspondingly reduced to 30µm. This Case 8 is illustrated in Fig. 6. As can be seen from Table 3, the fatigue life of the critical interconnection is further improved.

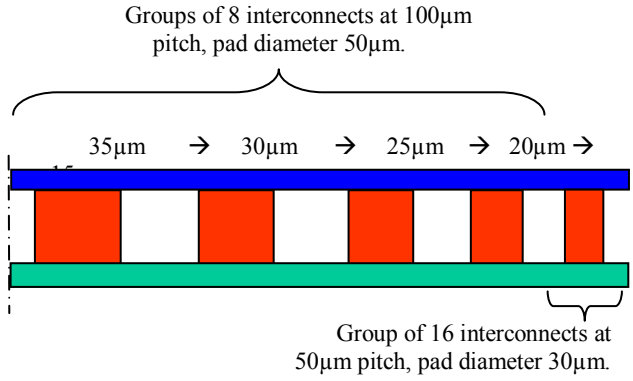


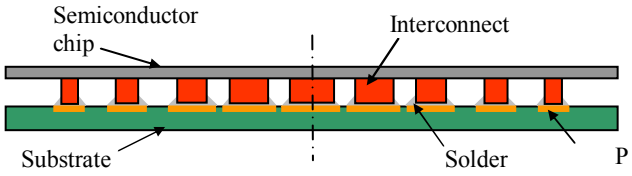
Fig. 6 Schematic illustration of interconnect geometries for Case 8.

Merits of Variable Compliance Interconnect Design

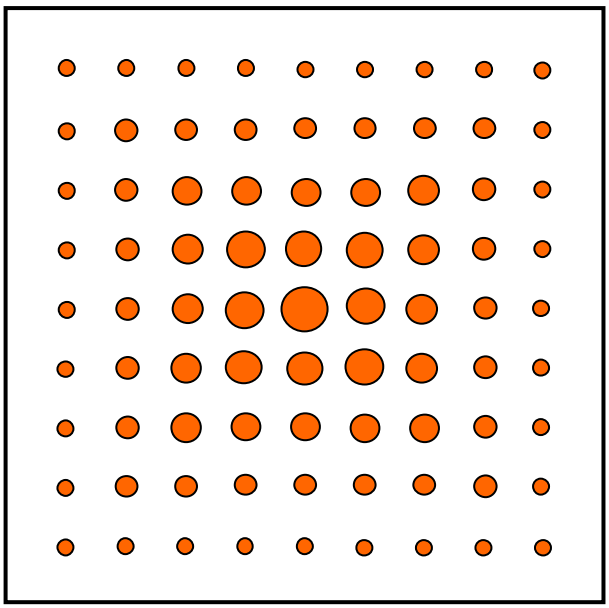
Fig. 7 shows a typical example of the variable compliance interconnect design for a flip-chip package. The interconnect shown in Fig. 7 is a copper pin or column interconnect. However, any other type of interconnect may be used including solder pins, stretched solder column and solder balls. As the diameter of the interconnects towards the perimeter of the package are smaller, the pad sizes can be correspondingly reduced. The reduced pad size have the additional advantage of facilitating the fanning out of metallization lines connecting the interconnects. This is illustrated in Fig. 8.

With this variable compliance interconnect design, the size of the interconnects towards the perimeter of the package are smaller. This allows for the specification of smaller pitches for the smaller size interconnects, if it is desired to increase the I/Os of the package. It was also shown earlier that this leads to increased solder joint reliability.

IEEE-CPMT and EIA, Orlando, FL, May 2005, pp. 545-550.



(a) Cross-sectional view across center of chip



(b) Plan view of interconnects on hi

Fig. 7 An example of variable compliance interconnect design.

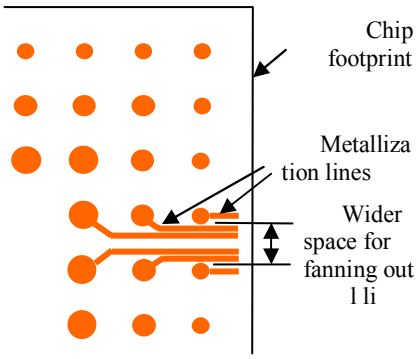


Fig. 8 Small pads lead to wider space for fanning out metal lines.

4. Conclusions

A parametric study of a copper column interconnect flip-chip package has been presented. Based on extensive finite element simulation studies, it has been demonstrated that if the compliance of the interconnect is increased with its distance from the center of the chip package, the fatigue life of the critical solder joint and hence the reliability of the chip package will be increased. By having such a variable compliance interconnect design, the stiffer interconnects nearer to the center of the chip are able to take up most of the CTE mismatch between chip and substrate, leaving the critical interconnect with a lower level of strain and hence a longer fatigue life. With the current method of fabricating copper column interconnects using a lithographic and plating process, the compliance of the interconnects can easily be varied.

A further improvement in package reliability can be achieved by also reducing the substrate pad size corresponding to the reduced diameter of the interconnects towards the perimeter of the package. The reduced pad size have the additional advantage of facilitating the fanning out of metallization lines connecting the interconnects. With this variable compliance interconnect design, the size of the interconnects towards the perimeter of the package are smaller. This allows for the specification of smaller pitches for the smaller size interconnects, if it is desired to increase the I/Os of the package.

Acknowledgements

The authors would like to acknowledge the support of the Nano Wafer Level Packaging Program which is a collaborative research project between National University of Singapore (NUS), Institute of Microelectronics, Singapore (IME) and Packaging Research Center, Georgia Institute of Technology, USA, funded by the Agency for Science, Technology and Research (A*STAR), Singapore, as a Temasek Professorship research project.

References

1. P. Borgesen and C. Y. Li, Mechanical design considerations for area array solder joints, Trans. IEEE, CHMT, vol. 16, no. 3, 1993, pp 272-283.
2. Kacker, K., Lo, G., and Sitaraman, S. K., Assembly and Reliability Assessment of Lithography-Based Wafer-Level Compliant Chip-to-Substrate Interconnects, 55th Electronic Components and Technology Conference,
3. D. Lau and S. W. R. Lee, Computational analysis on the effects of irregular conditions during accelerated thermal cycling tests on board level solder joint reliability, Proceedings of 6th Electronics Packaging Technology Conference, Singapore, December 2004, pp 516-521.
4. Y. T. Lin, C. T. Peng and K. N. Chiang, Parametric design and reliability analysis of wire interconnect technology wafer level packaging, Transactions of ASME, Journal of Electronic Packaging, vol. 124, pp 234-239, 2002.