

High-Speed Differential Interconnection Design for Flip-Chip BGA Packages

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Abstract

With the advancement of semiconductor technologies, packaging interconnect becomes one of the bottlenecks in high-performance devices. The paper deals with high-speed differential interconnect commonly used in the flip-chip ball grid array (Fc-BGA) packages. Layout issues for differential interconnect are first discussed, and the emphasis is put on the investigation on the effects of the discontinuity consisting of via and solder ball on electrical performance. Overall electrical performance of one typical differential pair is characterized and -15dB return loss and -23dB isolation between neighboring pairs are achieved up to 10 GHz. The purposes of this paper are to design and optimize high-speed series differential interconnects used in Fc-BGA packages with the first-round success.

1. Introduction

Today's telecommunications and consumer electronics are toward miniaturization, low power consumption, and high integration. Those trends in combination with increasingly higher transfer data rates place the challenges on interconnect design at all levels [1-3]. High-speed memory subsystem, full-buffered DIMM, is a good example, where multi-gigabit/s point-to-point serial differential interconnect is implemented among the advanced memory buffers and the host memory controller, which is being prominence for chip-to-chip communication.

In such a high-speed system, IC package becomes one of the bottlenecks and is responsible for the majority of signal degradation [4, 5]. On the other hand, the I/O number of packages increases with the increasing level of integration. Hence, it is necessary for package designer to develop broadband packaging solution within the frequency range from DC up to several gigahertz with several hundreds, even thousands, of I/O [6-8]. Furthermore, broadband packaging design must be carried out under much constraints as well as the short time-to-market requirement. The constraints include small escaping area, packaging manufacturability, limited material type, mechanical and thermal constraints, which make the design more challenging. Usually, they are also contradictory to electrical requirements, and the tradeoff must be made during packaging design. On the other hand, in order to reduce manufacturing cost, it is desirable to use conventional material and manufacturing process, however, which often have the negative impacts on packaging electrical, mechanical, and/or thermal performance.

The paper will focus on analysis and design of high-speed differential serial interconnect, used in low-cost, high-density, and high-speed Fc-BGA packages with conventional

manufacturing process. The purposes are to characterize electrical property and design differential series interconnects to promote its electrical performance. Firstly, layout issues are discussed, where impedance control for coupled transmission line is considered. The discontinuities like via and the related pads/antipad, and solder ball in differential interconnect have critical impacts on high-frequency performance, and must be carefully designed to meet specific electrical requirements. The paper takes the efforts on the analysis and design for them to achieve overall electrical performance of differential interconnect. Crosstalk between interconnects is another important signal integrity issue in high-speed and high-density packaging design. In the paper, differential-mode coupling between differential pairs is analyzed and characterized.

2. Layout Considerations

In high-speed and high-density flip-chip BGA package, it is critical to route the nets from solder bump to solder ball through package substrate, where packaging real estate is very scarce. It is well known that the interesting frequency range is completely determined by signal's rise/fall time, therefore the size of the concerned package and the length of interconnect are usually comparable to the interesting shortest wavelength. Hence, traditional lumped analysis is not enough and the distributed effects must be taken into account in electrical analysis, where the traces should be considered as the coupled transmission line with the controlled impedance. In high-speed substrate-based packages, the embedded coupled microstrip or stripline transmission lines are usually used for packaging differential interconnect, which normally have the length larger than one quarter of the shortest interesting wavelength. Therefore, the worst differential return loss [9] in a typical Fc-BGA package can be reached

$$RL_{\text{worst}} \cong 20 \log_{10} \left[\left| \frac{(Z^2 - Z_0^2)}{(Z^2 + Z_0^2)} \right| \right] \quad (1)$$

where, Z is the differential impedance to be achieved and Z_0 is the targeted differential impedance that usually is 100ohms for the most cases. It is assumed in Eq. (1) that Z is very close to Z_0 in its derivation. It should also be noted that it only takes impedance mismatching into account, that is, the transmission line is ideal and the effects of any discontinuities are not included. Fig. 1 shows the change of the worst return loss with the differential impedance error of interconnect, which is defined as $Error_{\text{imped}} = (Z - Z_0)/Z_0$. Roughly, -20dB to -25dB return loss requirement is met in the design depending on applications, which, in turn, permits about 5%–10% impedance mismatching, as indicated in Fig. 1. Differential

impedance mismatching in a practical package is due to manufacturing and material tolerance offset from the design. Fig. 2 shows how differential impedance mismatches the targeted value due to the relative manufacturing and material tolerance through 2D numerical simulations for a typical

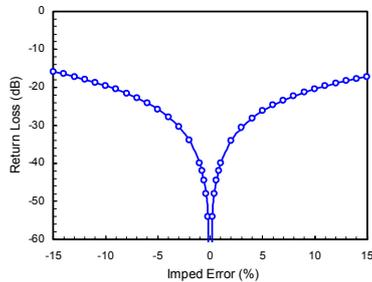


Fig. 1 The change of the worst differential return loss with differential impedance mismatching.

coupled stripline design in terms of dielectric constant (DK) and its height (height), trace width (width), trace thickness (thickness), and trace spacing (spacing). In the study, when one parameter changes, the others hold the nominal values

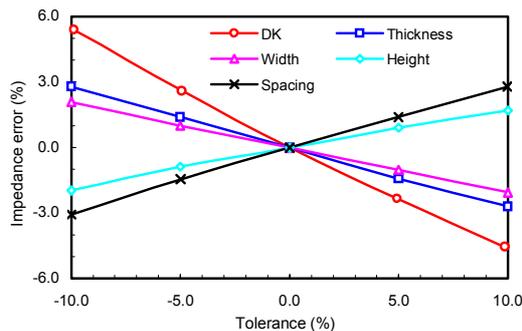


Fig. 2 Differential impedance changes with the tolerance of cross section size and material tolerance for a typical uniform centered stripline differential transmission line.

unchanged. It is found that the impedance changes linearly with all the relative tolerances, and DK tolerance has the greatest impact.

Solder bump area of a flip-chip BGA package has very limited escaping space, and therefore it is impossible to directly route normal differential interconnect. It is practical to implement compact differential pairs with small trace width and pitch, which sometime might be offset from impedance specification. However, because the escaping area is small, the length of this compact transmission line is only a very small fraction of the shortest interesting wavelength. According to the reference [10]

$$RL \cong 20 \log_{10} \left| \frac{(Z^2 - Z_0^2) \gamma l}{Z^2 + Z_0^2} \right| \quad (2)$$

$$RL \cong RL_{worst} + 20 \log_{10} |\gamma l| \quad (3)$$

The derivation of this equation assumes that γl is very small and the differential impedance z is very close to the nominal

impedance z_0 . The last term of the right side in Eq. (3) is negative under the above-mentioned assumption. For example, when the line length l is only one fiftieth of a wavelength, it contributes additional -18dB . Hence it is permissible to have impedance mismatching at this small area. The differential pairs with normal size are routed out of the escaping area.

In a practical package, it is impossible always to keep the differential transmission lines straight and symmetrical. In order to maximize electrical performance, it is important to have two traces with the same length for any differential pair. It is also desirable to keep their length as short as possible in packaging design.

3. Via Optimization

In differential interconnect analysis, the mixed-mode S-parameter is widely accepted, of which the detail can be found in reference [11]. We analyze and characterize packaging differential interconnect below in terms of this parameter using commercial software, Ansoft HFSS. In the paper, only the differential-mode results are presented due to limited space although the common-mode ones are also available.

Via and solder ball have the main contributions to return loss and insertion loss of differential interconnect, therefore, it is necessary to optimize them to improve high-frequency performance. It is well known that the staggered via has less



Fig. 3 Differential via together with solder ball studied here.

electrical performance than the stackup one because the former introduces more capacitive parasitic to internal power plane [9]. Vias in different layers are made using different manufacturing process with different size, among which the one in prepreg layer is usually fabricated with laser and the

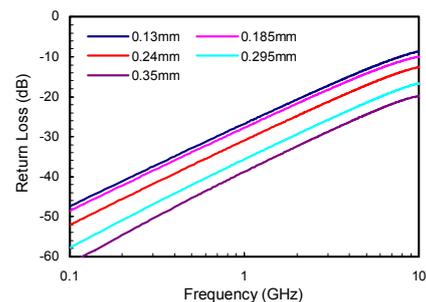


Fig. 4 Differential return loss changes with frequency at different via's antipad sizes in the layers 4&5.

one in core is fabricated mechanically. Its size, the related pads and antipads affect electrical performance. Below, we consider a 6-layer BGA package with the 800um-thickness core and 45um-thickness prepreg layers. A differential via to connect differential stripline transmission line in the 2nd layer to solder balls are studied, as shown in Fig. 3. It is desirable to use small-size via and pads, and large-size antipads to reduce

capacitive coupling to the power/ground plane. However, they cannot be changed arbitrarily due to manufacturability. One example is about solder ball, whose size and pitch is usually specified by standardization organization like JEDEC. The discussions will focus on the effects of different sizes and arrangements of a differential stackup via on electrical performance in terms of return/insertion loss under the manufacturing constraints by conventional low-cost process. The size of solder ball is fixed with the height, diameter, and pitch of 0.4mm, 0.52mm, and 0.8mm respectively. Therefore, in this stackup via, the sizes of pad and antipad are to be determined through the analysis.

3.1 The effects of via's antipad

In order to achieve the required performance, the effect of via's antipad is investigated. In the differential via mentioned previously, the radius of the antipads in layer 4&5 change

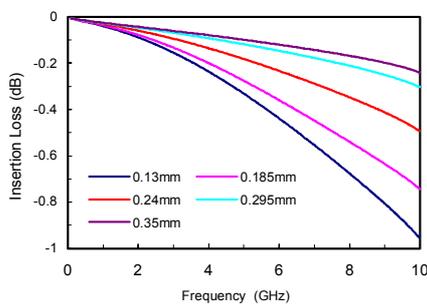


Fig. 5 Differential insertion loss changes with frequency at different via's antipad sizes in the layers 4&5.

from 0.13mm to 0.35mm while the one in layer 6 keeps the radius of 0.35mm unchanged. With the simulations from DC up to 10GHz, its differential return loss and insertion loss are shown in Fig. 4 and 5 respectively. It is found that differential

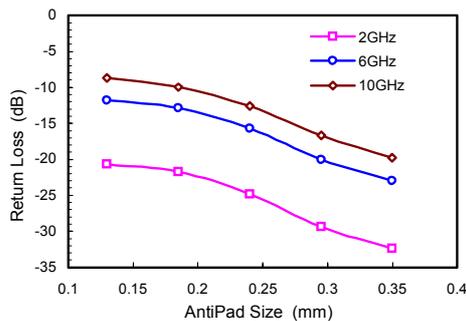


Fig. 6 Differential return loss changes with the size of via's antipad in the layers 4&5 at different frequencies.

return loss changes linearly with the logarithm of frequency and differential insertion loss decreases with frequency. Fig. 6 shows that differential return loss changes with antipad size at three frequencies, that is, 2GHz, 6GHz, and 10GHz. It is found that differential return loss changes slowly with antipad size at the beginning, and then changes rapidly with antipad size at the interval between 0.2mm to 0.3mm. After that, it changes slowly again. Consequently, it is better to have antipad size larger than 0.3mm in terms of electrical

performance. Fig. 7 shows the change of differential insertion loss with the antipad size at the frequencies of 2GHz, 6GHz,

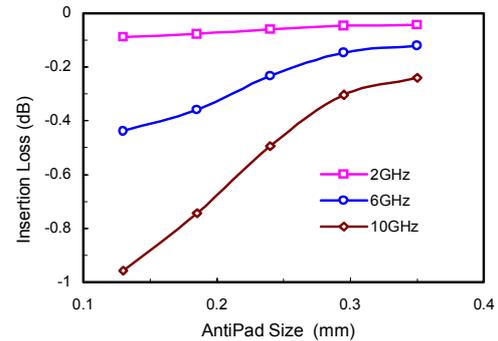


Fig. 7 Differential insertion loss changes with the size of via's antipad in the layers 4&5 at different frequencies.

and 10GHz. It is found that the insertion loss changes smoothly when the antipad size is larger than 0.3mm.

The above study combines the contributions from the antipads in the layers 4 and 5, however, the antipad located at different place has different electrical impacts. It is obvious that the antipad in the layer 5 has the greater impact as it produces much capacitive parasitic with the large via pad in the layer 6. Fig. 8 shows that differential return loss changes with the size of the antipad in the layer 5 whilst the radius of

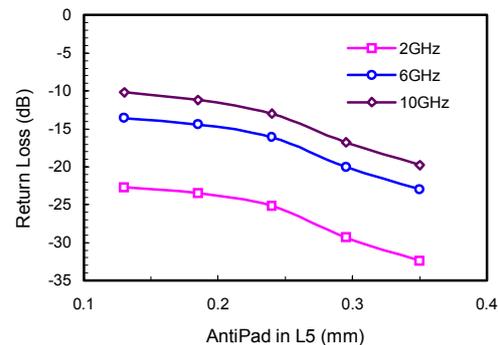


Fig. 8 Differential return loss changes with the size of via's antipad in the layer 5 at different frequencies.

the antipad in the layer 4 keeps 0.35mm unchanged. Compared with Fig. 6, it is found that with the radius decrease of the antipad in the layer 5, differential return loss increase, but slower than that both the antipads in the layers 4 and 5 change simultaneously.

Based on the previous discussions, the antipad with the radius of 0.35mm is a good choice for this differential via.

3.2 The effects of via's pad

Capacitive parasitic exists between via's pad and internal power/ground plane in the package, which deteriorates electrical performance. In order to reduce this parasitic, last subsection discussed the effect of via's antipad. Now the effect of via's pad is studied from DC up to 10GHz at different pad sizes. First, we study via's pad in prepreg of the layers 2 and 5 whilst the radius of via's pad in core holds 0.105mm. Differential return loss and insertion loss with the

change of frequency for different pad size are shown in Fig. 9 and 10. It is found that return loss changes linearly with the

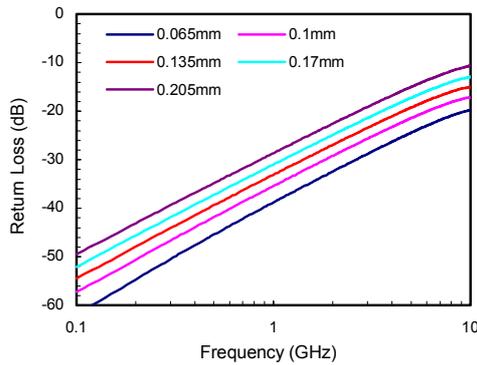


Fig. 9 Differential return loss changes with frequency at different sizes of via's pad in the layers 2 and 5.

logarithm of frequency, and insertion loss decreases with frequency. Fig. 11 and 12 show the change of differential

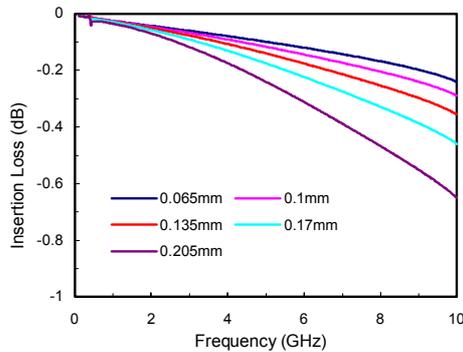


Fig. 10 Differential insertion loss changes with frequency at different sizes of via's pad in the layers 2 and 5.

return loss and insertion loss with via's pad size at the frequencies of 2GHz, 6 GHz, and 10GHz, where it is found that differential return loss increase almost linearly with pad

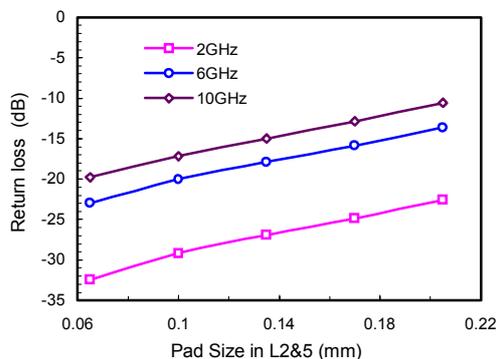


Fig. 11 Differential return loss changes with the size of via's pad in the layers 2 and 5 at different frequencies.

size, and therefore the increase of the pad size deteriorates its electrical performance. To achieve -20dB differential return loss at 10GHz, the radius of the via's pad must be less than

65um while it must be less than 135um if -15dB differential return loss at 10GHz should be achieved.

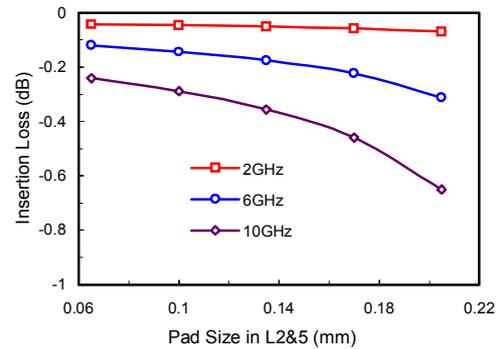


Fig. 12 Differential insertion loss changes with the size of via's pad in the layers 2 and 5 at different frequencies.

As mentioned previously, the via and the related pad in core and prepreg are different. The effect of the size of via's pad in the layers 3 and 4 is studied while the radius of via's pad in prepreg is assumed to be 65um. Fig. 13 shows the

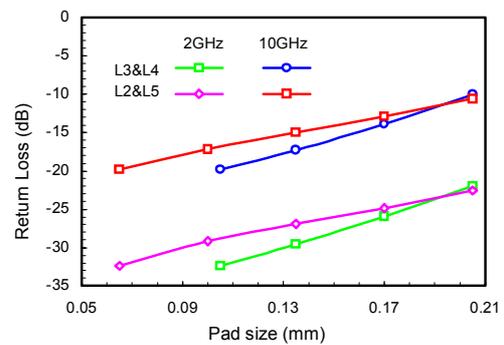


Fig. 13 Differential return loss changes with the size of via's pad in the layers 3 and 4 at different frequencies.

change of differential return loss with via's pad size at the frequencies of 2GHz and 10GHz. In order to compare the effects of different via's pad, the one due to the change of the size of the via's pad in prepreg is also shown in Fig. 13. It is found that the radius of via's pad in core must be less than 105um if -20dB is required and 160um for -15dB.

Based on the previous discussions, 65um and 105um are a good choice for the radius of via's pad in prepreg and core respectively, which takes the manufacturability as well as the required electrical performance into account.

4. Overall performance of differential pair

In last sections, layout issues, differential impedance control, and via are studied. However, differential impedance control is considered only under the condition of the perfectly coupled transmission lines. In the practical package, it is not straight due to limited packaging area. In addition, the reference planes above and below it are not integral, which definitely affect overall electrical performance of a differential pair in practical Fc-BGA package. Therefore, it is not enough only to carry out 2D analysis. Moreover, the effect of neighboring geometries is not included in previous studies.

Moreover, the interaction among the separate parts is also not taken into account. Therefore, it is necessary to carry out the overall analysis for typical differential interconnect. Fig. 14 shows a practical differential pair extracted from the design, where all the abovementioned concerns are included in this



Fig. 14 A differential pair used in a Fc-BGA package.

model, but the neighboring geometries and PWR/GND plane is not shown. In this differential pair, the traces are routed in the 2nd layer from solder bump with the compact centered coupled stripline at the beginning in the escaping area and then with the normal coupled stripline out of the escaping area. They are implemented with the differential impedance of

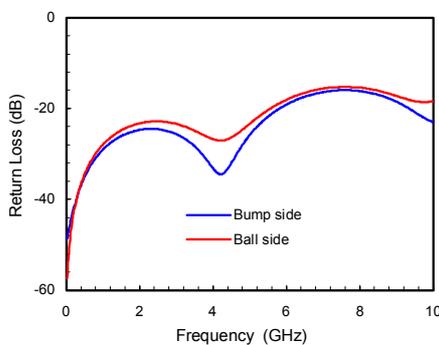


Fig. 15 Differential return loss for a good-designed differential pair used in practical Fc-BGA package.

100ohms. At the solder ball side, a differential stackup via is applied to directly connect the stripline in the 2nd layer and solder ball at the bottom of package, whose size was indicated in last sections. After 3D simulation, differential return loss for this differential pair is shown in Fig. 15 from DC up to

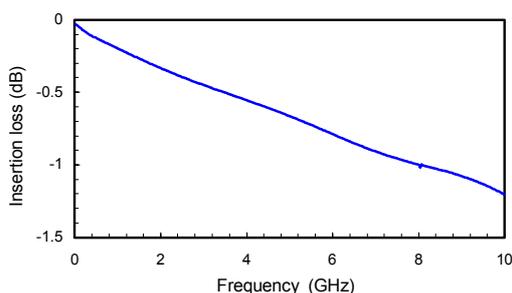


Fig. 16 Differential insertion loss for a good-designed differential pair used in practical Fc-BGA package.

10GHz at both solder ball and solder bump sides. After via design, the maximum differential return loss decreases within the frequency range from DC to 10GHz compared to that in [9], and less than -15dB differential return loss up to 10GHz is achieved. On the other hand, the frequencies at which maximum differential return loss reaches are shifted to higher end. From Fig. 15, the frequencies at the first and second

differential return loss peaks are 2.32GHz and 7.60GHz respectively compared to 2.2GHz and 7.3GHz before via design. Capacitive loading on transmission line is equivalent to lengthening its length. Through via design, its capacitive parasitic is reduced, hence the equivalent length of the differential pair shortens, therefore, the peaks move to higher frequency. Fig. 16 shows differential insertion loss of this differential pair, from which it is found that it decreases with frequency, and it is larger than -1.5dB from DC up to 10GHz.

5. Crosstalk

Crosstalk has become critical in high-speed Fc-BGA package due to its high density and high clock frequency/data rate. It is common that the spacing between neighboring traces gets smaller and smaller, which induces much differential-

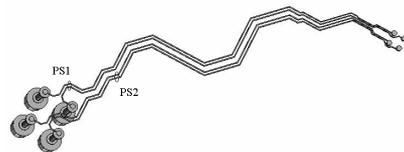


Fig. 17 Two differential pairs in crosstalk studies.

and common-mode coupling from neighboring interconnects. Although a differential receiver has the capability to cancel out common-mode noise, it is unable to immunize differential-mode noise. Hence, differential-mode noise

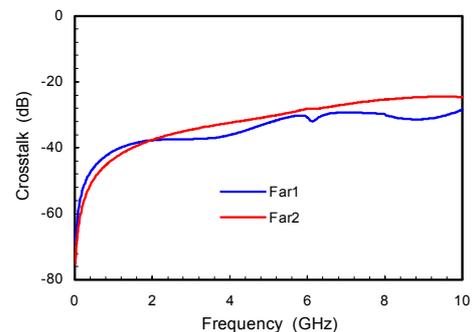


Fig. 18 Differential-mode far-end crosstalk between two differential pairs.

should be identified and suppressed in the design, otherwise signal quality will be degraded. For this purpose, two centered stripline differential pairs, as shown in Fig. 17, are studied for crosstalk through 3D simulations, where the differential pair PS1 is regarded as a victim, and PS2 is as an aggressor. The neighboring structures are also included although they are not shown in Fig. 17. The far-end crosstalk in terms of differential-mode S parameters is shown in Fig. 18, where Far1 indicates that the differential noise from the sold bump side of PS2 is coupled into the solder ball side of PS1 whilst Far2 means that the differential noise from the sold ball side of PS2 is coupled into the solder bump side of PS1. Fig. 19 shows differential-mode near-end crosstalk, where Near1 indicates that the differential noise from the sold bump side of PS2 is coupled into the solder bump side of PS1 while Near2 means that the differential noise from the sold ball side of PS2 is coupled into the solder ball side of PS1. It is found that

differential-mode crosstalk between PS1 and PS2 are all less than -23dB up to 10GHz for near-end and far-end crosstalk.

6. Conclusions

The paper takes the efforts on electrical characterization and design of high-speed Fc-BGA package with the emphasis on high-speed series differential interconnect. The key issues

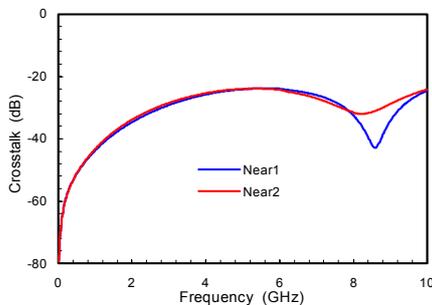


Fig. 19 Differential-mode near-end crosstalk between two differential pairs.

in differential interconnect design that have critical impacts on signal integrity are highlighted and studied, including layout issue, impedance control, via, crosstalk between differential pairs. 2D and 3D simulations are carried out to characterize their impacts on overall packaging performance. Material and manufacturing tolerances are also considered. Based on the studies, a typical differential pair used in low-cost Fc-BGA package is designed with electrical performance of less than -15dB differential return loss, larger than -1.5dB differential insertion loss, and less than -23dB differential-mode crosstalk up to 10GHz .

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