Package characterization of UTAC's Grid Array Package (GQFN) and performance comparison over standard laminate packages

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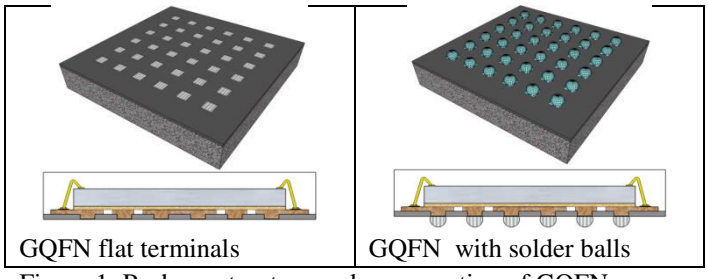
Abstract

The increasing demand and requirements for package with smaller footprint, higher dense I/O counts and better performance at lower cost are one of the key challenges faced by semiconductor manufacturing companies. As one of the strategies for sustainable competitive advantages and to address the issue, UTAC introduced a new generation of leadframe package design called Grid Array QFN (GQFN), where base material is leadframe but allows traces to be routed through etching process, hence providing higher I/Os that to date have required a two or four layers of laminate base packages. GQFN also has much smaller package form factor with reduction of package size up to 60%, shorter wire length with lower parasitic values and the feasibility to include a die attach paddle whilst having array of solder balls simultaneously. GQFN technology allows flip chip, stacked die, multi-chip module, passive integration and to meet the demand in leadless lead-frame applications. As part of package characterization, this package is subjected to comprehensive package analysis study using simulation and experimental data. In order to demonstrate the advantages and benefits of the package, this study projects the performance of GQFN to laminates package as a benchmark. Analysis methodologies and results of thermal, electrical and mechanical performance study will be discussed in detailed. From the comparative analysis study conducted, the overall thermal and electrical performance of GQFN is better than laminate packages. The package also has good results to meet the test requirement according to the IPC/JEDEC standards showing that the mechanical performance of GQFN is comparable to laminate packages.

Introduction

The GQFN package structure is similar to conventional QFN packages except that it has routed etched traces on the top half-etched lead together with the die attached paddle and multi-row or full array pad configurations on the bottom half-etched leads.



GQFN flat terminals | GQFN with solder balls

Figure 1: Package structure and cross section of GQFN

Figure 1 shows the package structure and cross section of the package with GQFN flat terminals and GQFN with solder balls. The GQFN package uses two types of mold compound where top mold is generic mold compound for conventional packages while the bottom mold called insulation mold compound has enhanced material properties to fill the tight clearance of the bottom half etched lead. This new innovative design was enabled with the advancement in process and materials technology within the industry.

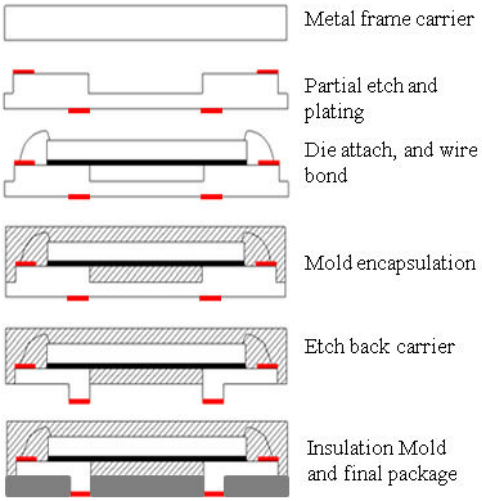


Figure 2: Major Process of GQFN packaging

The figure above illustrates the major process flow and area array configurations enabled with a routable lead-frame based technology. The metal frame is partially etched and pre-plated with either NiPdAu or selective Sn according to routed traces design. Followed by delivery to assembly line where die attach and wirebonding processes take place. The figure illustrated wirebond process but flipchip, stacked die and passive integration are supported as well. Once the front of line process is completed, the process continues with mold encapsulation process and post mold cure. After post mold cure, etch back of the leadframe carrier is performed to enable multi-row or full array I/Os pad configurations and complete the trace routing. [1] The package encapsulation is then completed with insulation mold process. Finally, printed solder bumps or ball drop for higher stand-offs can be performed before package saw singulation.

With the ability for the component being densely packed with routable traces and IOs array, there is flexibility to convert laminate base packages to GQFN as long as design is doable owing to line and space limitation, which can be

produced at a much lower or competitive cost compared to laminate packages.

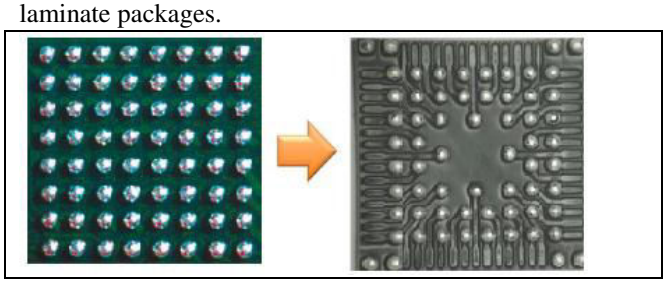


Figure 3: Conversion of laminate package to GQFN

GQFN has the flexibility to improve wiring diagrams to handle complex die pad layouts, multi or stacked die and SiP configurations. This design will have shorter wire lengths which will improve the electrical performance with lower inductance, capacitance and ultimately lower parasitic values. GQFN is a leadframe based package with the flexibility to include a die attach paddle whilst having array of solder balls simultaneously, as a result this package provides superior thermal advantage over laminates packages. In order to demonstrate the advantages and benefits of the package, package characterization and performance analysis of GQFN has been conducted. Simulations are executed to fully characterize the thermal, electrical and mechanical performance of GQFN to benchmark against laminates package and present the overall performance of GQFN.

Thermal Analysis

In order to assess the thermal effectiveness of the GQFN packages over laminate packages, both GQFN and FBGA packages are selected as test vehicles for evaluation. The test vehicles used in this study consist of extra-thin version of GQFN named xGQFN with the package size of 5 x 5 x 0.4mm and two layers substrate FBGA with the same package size. The package structure of the xGQFN is shown in the 3D model below. The model below shows an overview of the top mold, insulation mold, die attach paddle and the routed traces which connect to terminal pads.

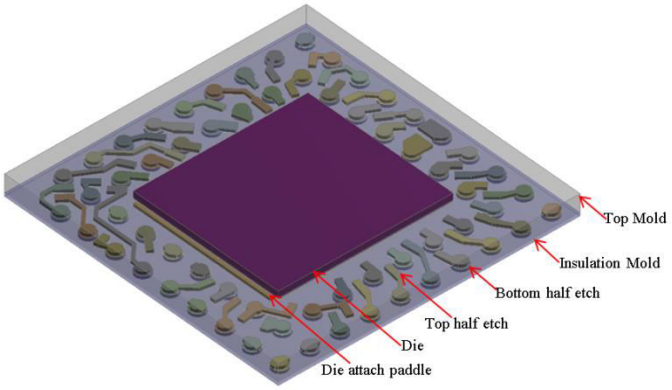


Figure 4: Package structure used in this study (xGQFN)

Thermal analysis using simulation was performed to evaluate and validate the thermal advantage over FBGA package in several test environments. Computational Fluid Dynamics (CFD) analysis method was adopted using the software FloTHERM to perform thermal simulation on both xGQFN 5x5mm 79L and FBGA 5x5mm 79B for a comparative analysis study. Package structure details for xGQFN 5x5mm are shown in the Figures below:

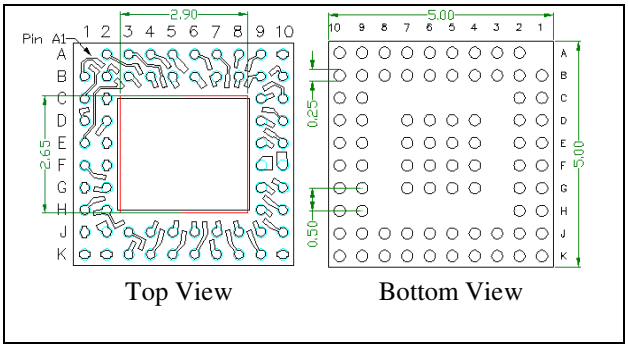
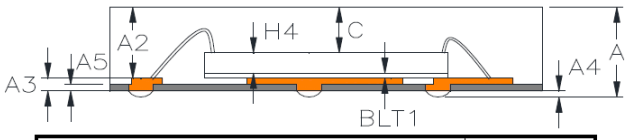


Figure 5: xGQFN 5x5mm 79L Top and Bottom View



PACKAGE THICKNESS (A)	0.450mm
MOLD CAP THICKNESS (A2)	0.25mm
LEADFRAME THICKNESS (A3)	0.101mm
DIE THICKNESS (H4)	0.100mm
BLT1	0.025mm
SOLDER BALL THICKNESS(A4)	0.100mm
POST MOLD THICKNESS(A5)	0.050mm
CLEARANCE BETWEEN TOP SURFACE OF DIE & MOLD CAP (C)	0.125mm

Figure 6: xGQFN package cross section /stackup

The overmold thickness is at 0.25mm which encapsulates over top traces, while the insulation mold is the same thickness as the bottom half etch. The leadframe thickness is at 0.1mm with top half etch at 0.05mm and bottom half etch at 0.05mm. There is a 3.0 x 2.5mm die paddle and this paddle is connected to 4x4 array of I/O pads. The die was backgrind to 0.1mm thickness.

In this study, both two layers substrate FBGA and GQFN package has the same power, die size and die thickness with some differences on the package structure due to package design nature such as substrate stack up/vias for BGA and the leadframe layout/thickness for GQFN. The substrate, leadframe and PCB traces are modeled as volume averaged layer with equivalent effective thermal conductivity. Radiation was applied to all the exposed surfaces which emissivity was assumed to be 0.8. [2] The percentage of copper on both layers is kept the same on both packages where layer-1 includes the percentage of copper from die paddle and traces/ leads and layer-2 includes package terminal pads. Package materials used are according to UTAC's standard bill of materials for BGA and GQFN packages. Localized grid cells were used to capture temperature profile and flow pattern in the areas of interest or where rapid changes are expected. [2] The packages are simulated in test environments which complied with JEDEC standards to acquire various thermal resistances; namely Junction to Ambient - Theta JA, Junction to Moving Air - Theta JMA(1m/s, 2m/s and 3m/s air flow),

Junction to Board – Theta JB and Junction to Case – Theta JC for comparison. The test environment used are JEDEC specified still air box for Theta JA as per JESD51-2A [3], forced air wind tunnel for Theta JMA as per JESD51-6 [4], ring cold plate set-up for Theta JB as per JESD51-8 [5] and top cold plate set-up for Theta JC. At the test environment for Theta JA, Theta JMA and Theta JB the package is soldered on a four layers JEDEC PCB (2S2P), while for Theta JC test, the package is soldered on a two layers JEDEC PCB (1S0P).

Both packages were simulated with the original design as well as the design of the packages without the 4x4 array of central balls below the die as a number of packages in production do not include central balls. This is in order to study the overall effect of thermal improvement from laminate package to GQFN with central balls and without central balls. Below are the results for this simulation.

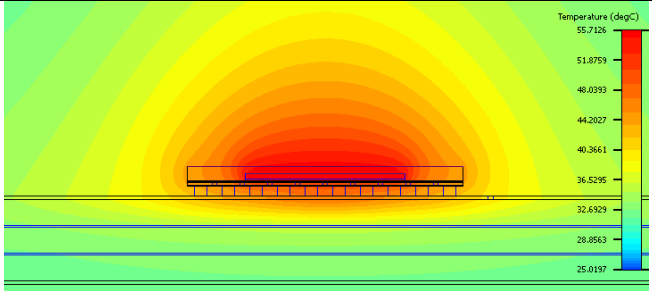
Thermal resistance	Air speed (m/s)	Package Type: BGA 5x5mm (degC/W)	Package Type: GQFN 5x5mm (degC/W)	% improvement
Theta JA	0	61.4	53.7	12.5%
Theta JMA (moving air)	1 2 3	52.6 51.0 49.9	46.2 44.7 43.7	12.2% 12.4% 12.4%
Theta JB	0	32.0	24.1	24.7%
Theta JC	0	11.7	10.7	8.5%

Table 1: Full thermal characterization result for BGA 5x5mm and GQFN 5x5mm with 4x4 array of central balls

Thermal resistance	Air speed (m/s)	Package Type: BGA 5x5mm (degC/W)	Package Type: GQFN 5x5mm (degC/W)	% improvement
Theta JA	0	69.1	58.4	15.5%
Theta JMA (moving air)	1 2 3	59.8 58.0 56.4	50.8 49.3 48.2	15.0% 15.1% 14.5%
Theta JB	0	39.3	28.4	27.6%
Theta JC	0	12.1	11.0	8.8%

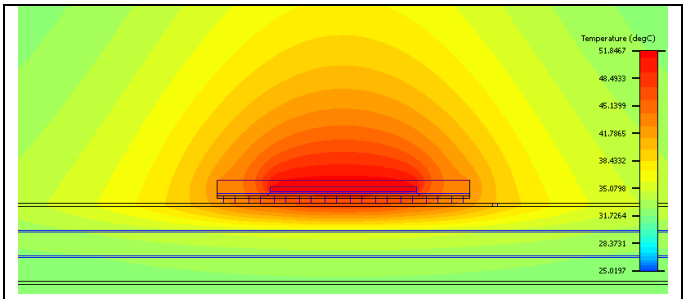
Table 2: Full thermal characterization result for BGA 5x5mm and GQFN 5x5mm without central balls

Below is an illustration of the temperature surface plot and distribution for both packages soldered on JEDEC 2S2P PCB under JEDEC still air condition. The hottest spot is at the center of the package.



Max temp: 55.7 degC at 0.5W

Figure 7: Temperature distribution around the package with 4x4 array of central balls. (BGA 5x5mm at Still Air Test on 2S2P PCB)



Max temp: 51.85 degC at 0.5W

Figure 8: Temperature distribution around the package with 4x4 array of central balls. (GQFN 5x5mm at Still Air Test on 2S2P PCB)

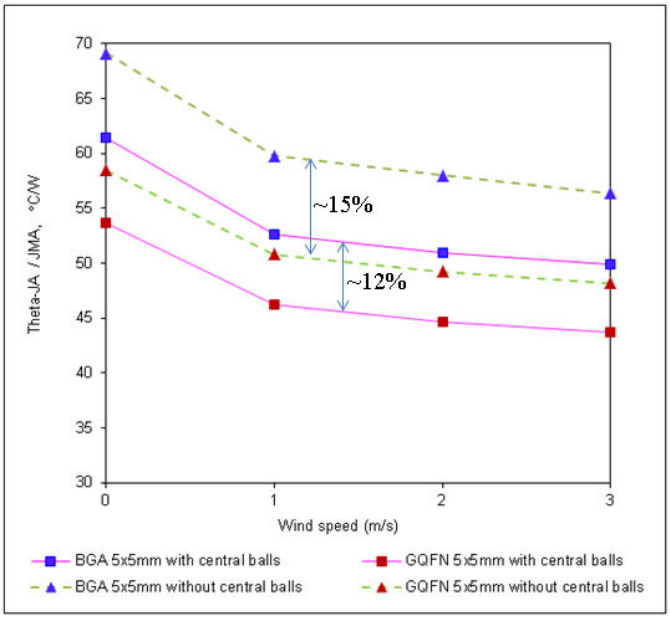


Figure 9: Thermal resistance Junction to Ambient/Moving Air versus Wind speed.

Package with lower thermal resistances will have better thermal performance. Based on this simulation, GQFN 5x5mm with 4x4 array central balls was shown to have significant improved thermal performance compared to FBGA package across all thermal resistances, summarized below:

a) 12.5% improvement in Theta JA thermal performance than FBGA, similar trend is observed for Theta JMA (1m/s, 2m/s and 3m/s)
b) 24.7% thermal improvement in Theta JB as compared to FBGA
c) 8.5% thermal improvement in Theta JC as compared to FBGA

As for the package without 4x4 central balls below the die, GQFN shows higher percentage of thermal improvement due to the higher impact of heat spreading effect of die attach paddle. From the above simulation results, it was shown that GQFN package has better thermal performance. This is mainly due to the direct conduction to the PCB via leadframe

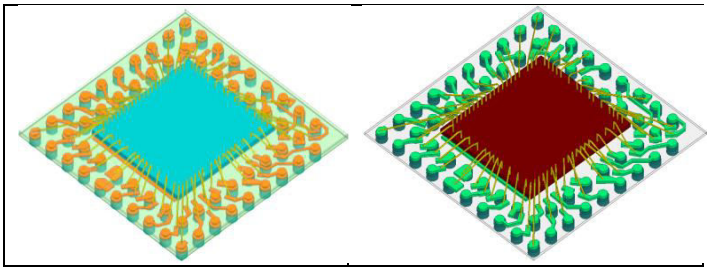
and solder and heat spreading effect of the die paddle, while for BGA package the heat is transferred from substrate layer-1 to layer-2 through limited substrate vias. Higher improvement on Theta JB is observed as the net heat flow or heat dissipation travel path is through package bottom to PCB. As a conclusion from this study, this new and innovative package GQFN has demonstrated clearly one of the advantages over FBGA in terms of thermal dissipation at a much more competitive cost.

Electrical Analysis

Both FBGA and GQFN 5x5 packages were submitted for electrical analysis. A parasitic extraction was performed in order to obtain the RLC (resistance, inductance and capacitance) values to compare its package performance at low frequency and S-Parameter simulation was conducted to be able to check each package performance at a higher frequency. Package assumptions used on the simulation are shown on the table below and parameters included on the simulation were based on JEP126 standard. [6] ANSYS Q3D Extractor was used to extract the parasitic values while Advance Design System (ADS) for the S-Parameter Simulation.

Item	GQFN	fBGA
Leadframe/Substrate Thickness (mm)	0.1	0.13
Wire Type/Loop height	25um Au/0.1mm	
Solder Ball (mm)	0.1	0.17

Table 3: Simulation consideration for the package



FBGA 3D view	FBGA 3D view

Figure 10: 3D view of both packages with wirebond

Figure 11 shows the extracted resistance, inductance and capacitance values for both packages. The higher parasitic value means lower performance. Based on the simulation results, there is no significant difference between the two packages. The electrical performance of GQFN package is as comparable to FBGA package at low frequency.

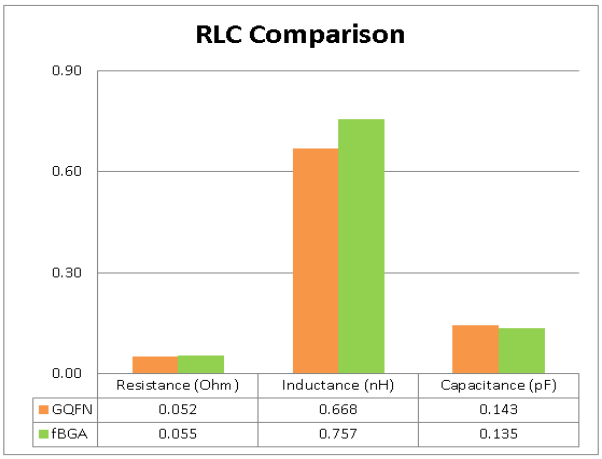


Figure 11: RLC comparison

S- Parameter Simulation was performed for high frequency analysis. A frequency sweep was performed on the longest span of a signal for each package. The GQFN package will have a good electrical performance up to 3.9GHz that is higher than FBGA package which is limited at 2.85GHz. Conditions used were -1dB limit for insertion Loss and -15dB for the return Loss.

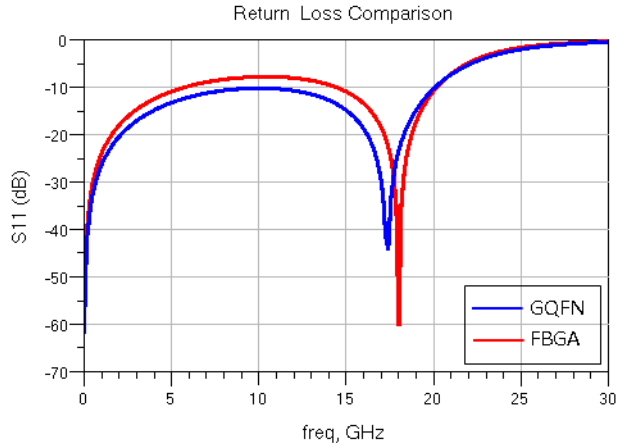


Figure 12: Return Loss

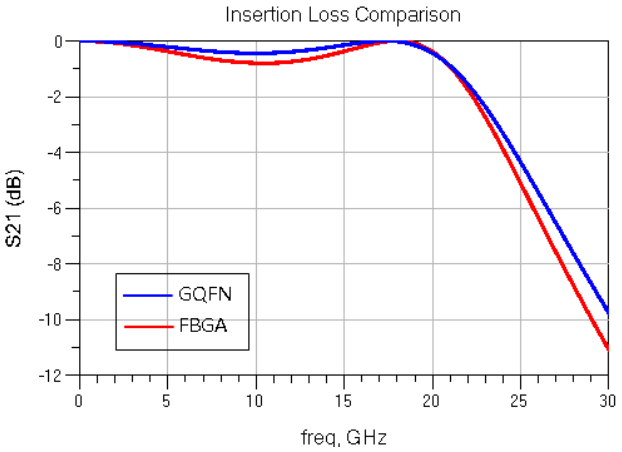


Figure 13: Insertion Loss

At low frequency, the electrical performance of the two packages is comparable. However, at higher frequency, the difference between the two packages can be seen and the GQFN package is better than FBGA package as FBGA

package's electrical performance deteriorate 1GHz lower than GQFN package.

Mechanical analysis on Board Level Reliability

Board level reliability analysis for the package xGQFN 5x5x0.45mm 79L with the die size of 2.9x2.6x0.1mm was conducted. High expectations for shock resistant mobile devices urged the industry to be compliance with the harsh test standards that requires up to 1,000 drop cycles. This requirement is a lot higher than JEDEC standard requirement of 30 drops. To conduct the board level drop test, xGQFN 5x5mm packages were mounted on 132x77x1.0mm 8-layers board which was designed to form an integrated daisy-chain with packages. The drop tester was used to evaluate the experimental board-level drop reliability evaluation. The test method is composed of free-fall dropping the board using a drop table from a specified height that corresponds to JEDEC Condition B (1500 Gs, 0.5 millisecond duration, half-sine pulse) as listed in JESD22-B110. [7]

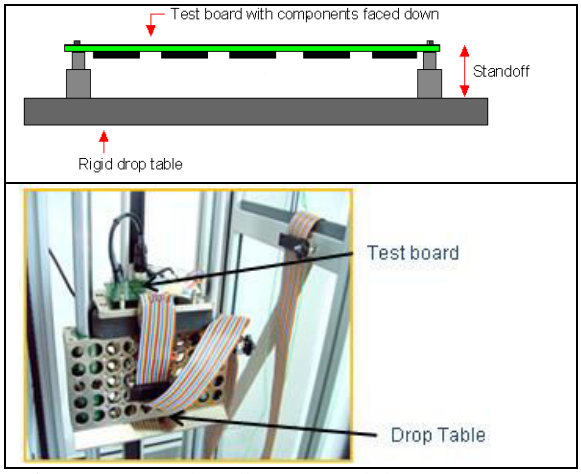


Figure 14: Test board mount and drop test setup

From the actual drop test result, the package xGQFN 5x5mm has shown excellent dropped performance with first failure at 470 cycles and characteristic life of 950 cycles that passed mobile customer's harsh test criteria. The characteristic life Weibull plot is shown in Figure 15 below.

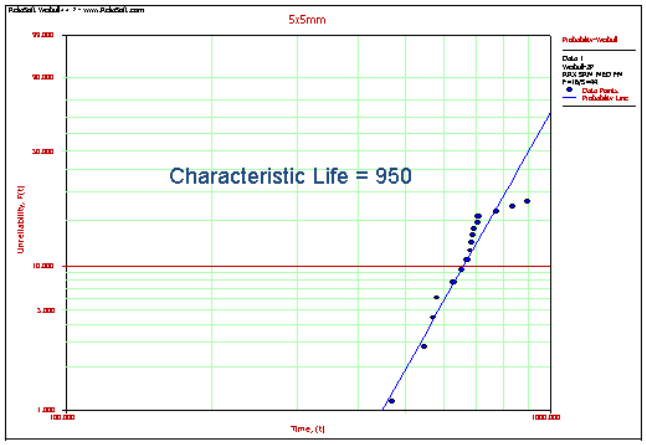


Figure 15: Weibull plot for drop test characteristic life.

Besides conducting actual drop test experiment, finite element (FE) modeling and simulation of the FBGA 5x5mm and xGQFN 5x5mm assembly with Pb-free solder were performed to investigate the stress-strain behavior of the solder joints during drop test. A 3-dimensional quarter FE model was used in this study with symmetric boundary conditions. Both FBGA and GQFN package have the same die size, die thickness, solder alloy and routings except different package thickness as in table below. The input acceleration of 1500G was applied onto the PCB support location. Sz stress density is extracted from top layer of the solder and the critical solder joint is at the package's corner. Both packages show similar stress density (FBGA: 114MPa vs. GQFN: 116MPa) and they are expected to have comparable dropped performance.

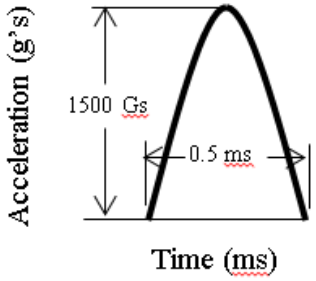


Figure 16: Input-G level

Dimension (mm)	XGQFN	FBGA
Mold cap	0.250	0.250
Leadframe/ Substrate	0.100	0.130
Solder standoff	0.100 (solder coat)	0.170 (solder ball)
Total package thickness	0.450	0.550
Die size (mm)	2.9 x 2.6 x 0.1	2.9 x 2.6x 0.1
SZ stress density (MPa)	116	114

Table 4: Assumption details and result

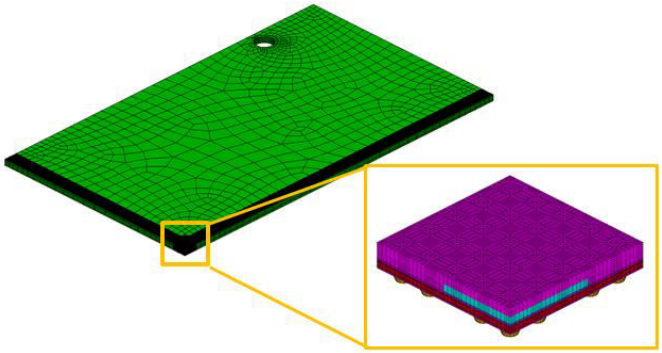


Figure 17: Quarter PCB model

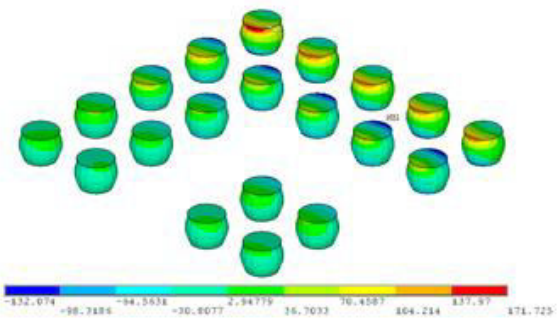


Figure 18: Solder joint stress density

GQFN design has much smaller package form factor with reduction of package size up to 60% owing to routable leads and full grid array capability. Increasing die to package ratio poses concerns on board level reliability as silicon is well-known to be the major source of CTE mismatch between package and PCB. xGQFN 5x5mm packages were attached to 200x150mm board and subjected to accelerated life tests to determine their second level reliability. TCoB chamber was used to evaluate the board-level reliability of the package under temperature cycling range of -40ºC to 125ºC, 15min dwell/soak time, 15min ramp, 1 cycle per hour according to IPC-9701A standard. [8]

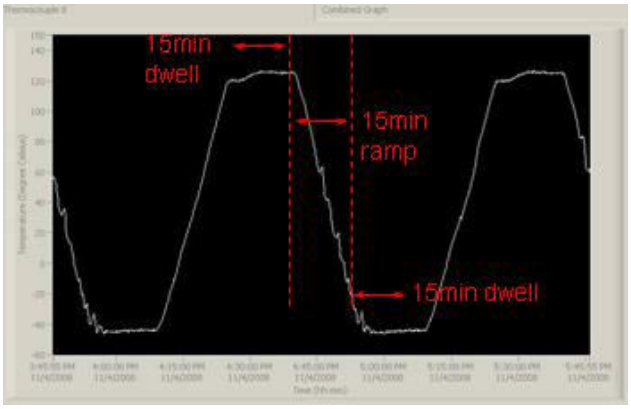


Figure 19: TCoB temperature cycle profile

Weibull plot showing the characteristic life which is the life cycles at which 63.2% of the test components have failed. Albeit die to package ratio is 58%, xGQFN 5x5mm had excellent TCoB performance with first failure at 2,680 cycles and characteristic life of 4,600 cycles.

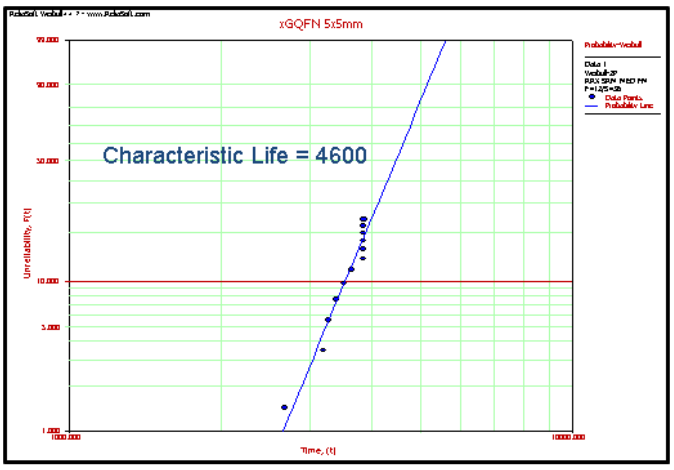


Figure 20: Weibull plot for TcOB characteristic life.

Package Level Reliability (1st Level)

Experimental moisture sensitivity level (MSL) test and accelerated moisture resistance –unbiased HAST (uHAST) were performed on the same xGQFN 5x5mm 79L package used for thermal, electrical and mechanical analysis. Moisture sensitivity level test is to identify the classification level of non-hermetic package that are sensitive to moisture-induced stress. xGQFN 5x5mm passed MSL 1 with test condition of 168hours, 85°C/85% RH as per IPC/JEDEC J-STD-020D standard. [9] uHAST is performed to evaluate the reliability of non-hermetic packages in humid environments. It is a highly accelerated test which employs temperature and humidity conditions to accelerate the penetration of moisture to identify package's internal failure mechanisms. The GQFN package passed the uHAST at the test condition of 130°C/85% RH, both 96Hrs & 192Hrs as per JESD22-A118A standard. [10] The package reliability test results are summarized in Table 5 below.

	Test Condition	Specifications	XGQFN Package 5x5mm
1st Level Reliability			
Moisture Sensitivity Level Test	J-STD-020D.1, MSL1	168hrs, 85C/85% RH	Passed
Unbiased Temp/Humidity (uHAST)	JESD22-A118	130C/85% RH,96Hrs/192Hrs	96 Hrs--Passed 192Hrs--Passed
2nd Level Reliability			
Drop Test	1500G, half sine pulse, 0.5ms	30 drops min	Passed
TCoB	-40C to 125C	1000X	Passed

Table 5: Summary of reliability test results

Conclusions

The innovative design of GQFN has provided the company with several advantages and benefits such as lower packaging cost and better package performance. In this study, thermal simulation was performed to study the thermal performance of GQFN using FBGA package as a benchmark based on JEDEC standards. From the analysis, the thermal performance of GQFN is better than FBGA for Theta JA, Theta JMA, Theta JB and Theta JC due to the direct conduction to the PCB via leadframe and solder as well as heat spreading effect of the die paddle. The electrical performance of GQFN package is comparable to FBGA package in low frequency applications. However, GQFN is better in high frequency applications as FBGA package's electrical performance deteriorates earlier. FBGA application frequency range is 1GHz lower than GQFN package. Mechanical simulation analysis also showed that both GQFN and FBGA have comparable board level dropped performance. The GQFN packages passed all board level reliability as well as package level reliability requirements in accordance with IPC/ JEDEC standards and the packages were qualified.

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