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Drop impact reliability testing for lead-free and lead-based soldered IC packages

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Abstract

Board-level drop impact testing is a useful way to characterize the drop durability of the different soldered assemblies onto the printed circuit board (PCB). The characterization process is critical to the lead-free (Pb-free) solders that are replacing lead-based (Pb-based) solders. In this study, drop impact solder joint reliability for plastic ball grid array (PBGA), very-thin quad flat no-lead (VQFN) and plastic quad flat pack (PQFP) packages was investigated for Pb-based (62Sn–36Pb–2Ag) and Pb-free (Sn–4Ag–0.5Cu) soldered assemblies onto different PCB surface finishes of OSP (organic solderability preservative) and ENIG (electroless nickel immersion gold). The Pb-free solder joints on ENIG finish revealed weaker drop reliability performance than the OSP finish. The formation of the brittle intermetallic compound (IMC) Cu–Ni–Sn has led to detrimental interfacial fracture of the PBGA solder joints. For both Pb-based and Pb-free solders onto OSP coated copper pad, the formation of Cu_6Sn_5 IMC resulted in different failure sites and modes. The failures migrated to the PCB copper traces and resin layers instead. The VQFN package is the most resistant to drop impact failures due to its small size and weight. The compliant leads of the PQFP are more resistant to drop failures compared to the PBGA solder joints.

1. Introduction

Portable electronic products such as cellular phones, digital cameras, and MP3 players are growth areas for the electronics manufacturing industry. The product and packaging design trends continue to push for smaller form factor and increased functionalities. Portable electronic products are prone to accidental drops and can cause internal circuit board damage, for example, solder joint failures by brittle fracture at the solder joint intermetallic compound (IMC) interfaces or by impact fatigue in the solder materials. If the solder joint is robust, the failure site can migrate to the board copper traces or even resin cracking. When an electronic product drops on the ground, impact force and deformation is transferred internally to the printed circuit board (PCB), solder joints and the Integrated Circuits (IC) packages. The IC packages are susceptible to solder joint cracks, induced by a combination of PCB bending and mechanical shock inertia during the impact event. If a single drop event does not cause failure, repeated drop

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events can cause impact fatigue or accumulated damage and rupture of interconnection joints and assembly materials. Drop testing provides a useful experimental approach to design for drop reliability. From the physics of failure characterized in the drop test, improved solutions to IC package design can be implemented to avoid such drop-related failures in service. Research on drop impact testing and finite element modeling investigations [1–13] are further needed for developing a design-for-reliability (DFR) methodology [5] for drop impact reliability qualification of board-level soldered assemblies. Drop impact responses such as acceleration and strains experienced by the PCB are obtained and studied to investigate the mechanisms of the solder joint failure modes.

Pb-based solders (63Sn–37Pb, 60Sn–40Pb, 62Sn–36Pb–2Ag) have been employed in the electronic industry for four decades. Pb-free solders will replace Pb-based solders. The Sn–Ag–Cu alloy is a popular choice for replacement of Pb-based solders, but there are concerns on its solder joint reliability performance subject to drop impact testing. More experiments and numerical analysis are required for Sn–Ag–Cu solders in the range of Sn–(3–4)Ag–(0.5–1)Cu.

Studies were already conducted on the effect of PCB surface finish (e.g. ENIG or OSP) on the thermal fatigue reliability performance of Sn–Ag–Cu solder joints and its underlying failure mechanism. However, the influence of surface finish on drop impact reliability has not been readily documented and the failure mechanism needs further characterization. This study investigates the effect of drop impact test on the reliability of solder interconnects of Pb-based (62Sn–36Pb–2Ag) and Pb-free (Sn–4Ag–0.5Cu) solder compositions. Several package types and two different PCB surface finishes of OSP and ENIG were evaluated. Test vehicles used are 35 mm × 35 mm 312 balls PBGA (plastic ball grid array), 28 mm × 28 mm 208 leads PQFP (plastic quad flat pack) and 7 mm × 7 mm 48 leads VQFN (very-thin quad flat no-lead) packages with daisy chain interconnects for continuous monitoring of the solder joint resistance during drop impact testing. The failure site, modes and mechanism are reported in this paper.

2. Drop impact test failure mechanisms

From product level drop test reported by Lim et al. [3], it was found that a horizontal drop orientation gives the largest impact responses. Wong et al. [2] identified three board-level drop impact characteristics; (a) elongation and bending of interconnection due to differential flexing of PCB and package, (b) inertia force from electronic packages, and (c) longitudinal stress wave from impact. Due to the variation in stiffness of the IC package and the PCB where it is being mounted onto, it results in different flexing of the package and PCB when the board is subjected to a horizontal drop impact. For a package mounted at the centre of the PCB, this differential flexing has caused the corner solder joints to experience the largest tensile stress that leads to detrimental failure.

Inertia force of a body is the second driver for interconnection failure. During free fall, the IC package travels at the same velocity with the PCB mounted onto. Upon horizontal impact, an IC package with a larger size (thus larger mass) will experience a larger inertia force where force = mass × acceleration. As a result, the solder interconnects fall apart when the impact force reaches a threshold limit. The location of the package on a PCB plays a part in the solder interconnect strength as well. The PCB adjacent to the supports could experience up to a thousand times (1000*g*) acceleration and a package near to it could also experience the same acceleration. For a package at the center on the same PCB, its acceleration could only be in the range of hundreds of gravitational acceleration. Thus given the same mass, interconnects in the package placed near the support will be subjected to a larger tensile stress and eventually more prone to impact failure. Lastly, the high magnitude of longitudinal stress waves transmitted from the support to the adjacent interconnects may induce failure in it.

3. Drop impact testing experimental setup

The test packages were assembled on a 150 mm × 200 mm PCB (see Fig. 1). The solder compositions used in the test are: Pb-based of 36Pb–62Sn–2Ag for PBGA packages and 15Pb–85Sn for the PQFP/VQFN plating, Pb-free of Sn–4Ag–0.5Cu (also known as SAC) for PBGA packages and matte pure tin for the PQFP/VQFN plating. Solder paste used for all packages during board assembly were 36Pb–62Sn–2Ag and Sn–4Ag–0.5Cu for Pb-based and Pb-free legs, respectively. The

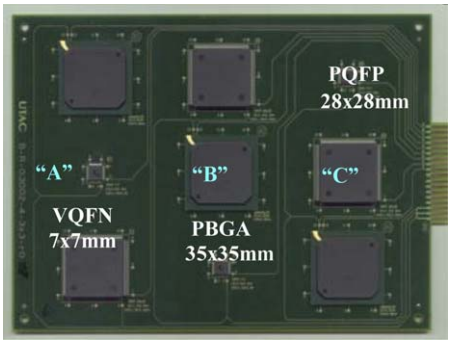

Fig. 1. 150 mm × 200 mm PCB with assembled drop test IC packages.

test legs with different pad surface finishes were broke down as (i) Leg 1—Pb-free solders on ENIG pad finish, (ii) Leg 2—Pb-free solders on OSP pad finish, and (iii) Leg 3—Pb-based solders on OSP pad finish. The fabrication process of different finishes is briefly described. For ENIG pad finish, the bare copper PCB is first dipped into a plating bath of nickel–phosphorous (Ni–P) alloy at temperature of 86–90 °C for approximately 20 min. The P content of 6–8 wt.% acts as a reducing agent for electroless plating of the nickel onto the copper surface, which will also be co-deposited in the nickel layer. The immersion gold process is next followed by immersing the nickel surface into a potassium gold cyanide solution. The immersion process is an ion-exchange process in which a metal ion in solution is reduced to the metal at the expense of the surface, which is oxidized to an ion. The exchange process is one directional only depending on the galvanic potential difference between the interacting metals. In this case, the gold ions from the solution are reduced to gold metal by taking the electrons from the nickel layer, and the immersion deposition will stop once the nickel surface is fully covered by gold. Hence, the immersion gold process is self-limiting, thereby preventing excessive thickness of gold from being deposited. Based on the PCB vendor's capability, a consistent thickness of 5 μm (±2μm) of nickel layer is plated over the copper pads. The immersion gold layer is appropriately 0.05 μm (±0.02μm). The nickel layer provides a good barrier preventing the copper from being diffused into the solder joints, where detrimental growth of Cu–Sn intermetallic is prohibited. The outermost gold layer offers good wetting and preventing corrosion in the underneath layers. The OSP surface finish is formed by coating a layer of benzimidazole compounds over the PCB copper pads. A commercial grade of Entek Plus CU-106A is used in this study with a coating thickness of 0.35 μm (±0.15 μm). During solder reflow, the gold layer dissolves rapidly into the solder and the nickel barrier layer forms a metallurgical joint with the solder. As for the OSP coating, it is evaporated and allows the interaction of the solder with copper forming metallurgical joints.

The Lansmont Model 65/81 drop impact tester (see Fig. 2) was used to conduct the test. Six boards (sample size) were dropped for each three legs. The PCB drop orientation is horizontal with packages in a face-down position. The PCB is mounted along the length-wise direction in a clamp–clamp position onto the aluminum fixture where it is fixed to the drop table (see Fig. 3). During the test, the drop table is raised and dropped from a desired height of 1.0 m along the two guiding rods of the drop tester onto a rigid base covered with one layer of felt pad. Upon impact, the drop responses of interest are the shock level experienced by the PCB and the IC packages, the strains experienced at the center of the PCB, and the static and dynamic resistances of

Fig. 2. Lansmont model 65/81 drop impact tester.

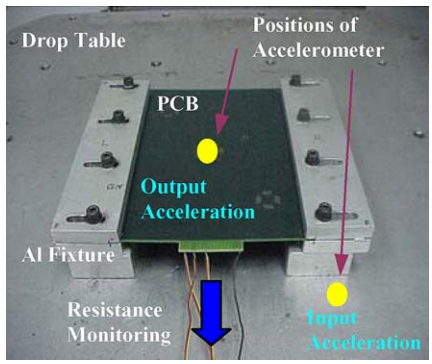

Fig. 3. Drop test fixture with PCB mounted onto it.

daisy-chained solder joints in real time. As the PCB is experiencing maximum bending at the center during drop, only packages labeled "A", "B" and "C" along the centerline of the board will be monitored for drop impact failure. Referring to Fig. 3, an accelerometer is mounted on the drop table near to the fixture to measure the input acceleration. Another accelerometer is mounted at the center of the PCB (reverse side of the IC package) to characterize the output acceleration response of the PCB. The accelerometers are connected to charge amplifiers and a data acquisition system with TP3 software to monitor the acceleration readings. The peak input shock pulse of the drop table was about 560 g in the form of a half-sine shape with 2 ms period as shown in Fig. 4a. With stress waves transmission from the drop table though the support, the dynamic response of the PCB center after impact is approximately doubled to 1000 g (see Fig. 4b). Strain gauges were mounted on the PCB at the opposite side of the center PBGA package to measure the bending strain experienced during drop impact. A data acquisition setup was used for strain measurements. It consisted of strain gauges arranged in a Wheatstone bridge circuit of a half bridge connection, a dynamic strain meter (TML DC-92D) and

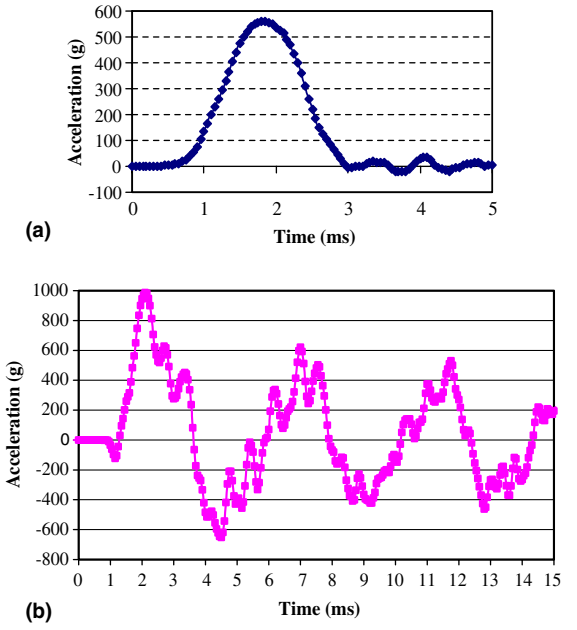

Fig. 4. Acceleration measurements upon drop impact. (a) Input acceleration at the drop table. (b) Output acceleration at the centre of PCB.

a digital oscilloscope (Yokogawa DL-1540). The signals from strain meters are linked to the oscilloscope. For drop test consistency and repeatability, drop responses of input/output acceleration and PCB strain were monitored for one board from each leg. Both the acceleration and strain values were found to be reproducible.

In many cases, event detectors are recommended for continuous monitoring and detection of the solder interconnects connectivity failure. However, event detectors setup is expensive and with its ability of registering only an event (e.g. failure with resistance reaches 300 Ω or more), it may not be able to capture the continuous intermittent failure occurring in a solder joint. The dynamic resistance measurement of daisy-chained solder joints in real-time during drop impact is used [6]. According to Luan et al.'s method, a resistor, R_0, is placed in series with the daisy chain solder joints and connected to a DC power supply. The dynamic resistance of solder joints, R_x, can be described by

$$R_x = \frac{R_0 V}{E - V} = \frac{R_0}{E/V - 1} \quad (1)$$

where E is the voltage (1.8 V) of the DC power supply, and V is the dynamic voltage of daisy chain that changes with the dynamic resistance of the daisy chain. In this way, the voltage is monitored instead of the resistance using an oscilloscope. When $V \to E$, $R_x \to \infty$ (which implies an open circuit), it indicates the critical solder joint has failed with crack opening. R_0 of 10 Ω was used in this test.

4. Results and discussion

The current test vehicles have undergone thermal cycling test of −40 °C to + 125 °C with 1 cycle/h for joints' integrity assessment under thermo-mechanical loading. All three legs had survived 1000 cycles of thermal loading, thus implying that the component mounting reflow profile was optimized for reliable solder joints formation. A total of 50 drops was conducted for every PCB. Before drop, the solder joint resistance was measured by manual probing to ensure no failure in the interconnection was observed. It is common to observe that the solder joint crack opens up resulting in a resistance discontinuity during drop impact and closes back to resume electrical continuity after the flexing of the board has ended. This observation is due to the upward/downward flexing of the PCB leading to the opening/closing mode of the crack. This is known as an intermittent solder joint failure where static resistance measurement by manual probing is not able to register any discontinuity. When the crack becomes larger and cannot be closed back even after the impact test, a permanent solder joint failure will be resulted (open circuit registered with static resistance measurement). In the current test, the permanent solder joint failure is identified as the failure criteria.

4.1. Drop impact dynamic responses

The dynamic resistance of the daisy-chained solder joints in real-time during drop impact is represented by a voltage reading on the oscilloscope. In any drop, the solder joints resistance (or "voltage") for the three packages and PCB bending strain were captured. A typical response curve is showed in Fig. 5 where it can be divided into two regions, before impact (static) and after impact (dynamic). Before impact, the PCB strain is zero while the static solder joint resistance is similar to the

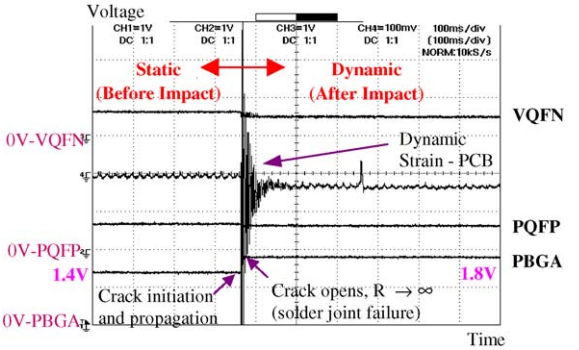

Fig. 5. Dynamic responses for Leg 1 (Pb-free on ENIG) test board at first drop.

value measured by manual probing. Each package has its own zero-reference voltage and initial voltage reading as indicated. One large division in the y-axis of the oscilloscope corresponds to 1.0 V. During the first drop of test board in Leg 1 (Pb-free on ENIG), dynamic strain was recorded due to PCB bending after impact. In channels 1 and 2 for VQFN and PQFP, respectively, there were little changes in the resistance responses before and after the impact, indicating that no solder joint failure has occurred.

For channel 3 (PBGA component), the resistance increased sharply from an initial value of 1.4 V [R_x (initial) = $10/(1.8/1.4 - 1) = 35\ \Omega$] to 1.8 V [$R_x$ (final) = ∞] and remained at that level as seen in the dynamic response curve. This indicated that an open in the connectivity has been detected (probably due to a solder joint crack). The discontinuity was confirmed by manually probing again of the resistance connectivity. An open circuit was measured, thus implying that the joint opening is permanent. It is to note that the failure corresponded with the highest dynamic strain value as shown. The subsequent drop for other test boards in Leg 1 revealed that most of the PBGA joints failed within a maximum of six drops. Failure analysis was done and solder joints cracks were observed by cross sectioning the samples. Details of the failure analysis will be reported in the subsequent section.

The drop dynamic responses for Leg 2 test vehicles (Pb-free on OSP) are illustrated in Fig. 6. With the Pb-free PBGA solder balls mounted onto an OSP pad finish, the first failure was observed at the 15th drop. From the graph, the resistance was again increased from an initial value of 1.4 to 1.8 V after impact. However, some differences in the response were noted against Leg 1. In contrast to Leg 1, the dynamic resistance did not reach the 1.8 V level immediately but fluctuates for a short period of time before reaching 1.8 V permanently. This observation was first postulated that upon impact, a solder joint crack was initiated followed by

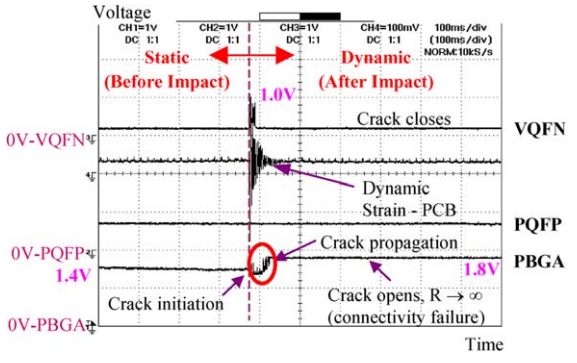

Fig. 6. Dynamic responses for Leg 2 (Pb-free on OSP) test board at 15th drop.

a rapid crack propagation till total failure (dynamic resistance reaches infinity, $V \rightarrow E = 1.8$ V). Manual probing after the drop confirmed that the static resistance reached infinity and hence permanent failure was registered. Cross sectioning showed that no solder joint crack was found. Copper trace failure was observed instead. From the dynamic curve response, the copper trace fatigued after 14 impact drops. At the 15th drop, the copper trace tear in a ductile manner and the failure was not immediate. With subsequent PCB flexing, it caused the copper trace to rupture and resulted in a permanent connectivity failure. The above failure mode shows that Pb-free Sn–4Ag–0.5Cu solder with OSP pad finish gives a much stronger joint durability to drop impact test than the case with ENIG surface finish.

As for the VQFN package, some intermittent failures were observed in the dynamic resistance curve. Crack in the VQFN interconnects has started to initiate and propagate through the joint interface at the 15th drop. However, the crack was only partial, hence the resistance peaked to about 1.0 volt (instead of 1.8 V which indicates total crack opening). When the PCB bends downwards, the outermost solder joints are subjected to tensile stress thus leading to an open mode in the crack. On the other hand, when the board bends up, the joints are under compression which helps the crack to close up. Towards the end of a drop, the partial crack would most probably closes up when the flexing of the board is over. At this instance, manual probing after the drop test would not register any failure. As such, no failure was considered for the VQFN package after the 15th drop. When probed manually, the static resistance after drop is 7.1 Ω as compared to a static resistance of 5.1 Ω before drop. No change in the resistance response was observed for PQFP after the impact, indicating again that no interconnect failure has occurred.

Failure mode similar to Leg 2 was observed in Leg 3 where 36Pb–62Sn–2Ag solder balls were mounted onto an OSP pad finish. Failure analysis showed that the interconnection failure was due to copper traces breakage and not solder joint crack. Fig. 7 shows some intermittent failures (resistance peaks) were observed for the PBGA package in the dynamic resistance curve at the 39th drop. The copper trace crack was completely opened at the resistance peaks ($V \rightarrow E = 1.8$ V). However, the gap of the crack may be small and the crack surfaces came into contact again after the impact. Manual probing after 39th drop registered good connectivity. At the 40th drop, the PBGA package registered a constant dynamic resistance of $V = 1.8$ V. Manual probing after the drop confirmed permanent failure. Lastly, no change in the resistance response for VQFN and PQFP indicated that no interconnect failure was recorded after 40 drops.

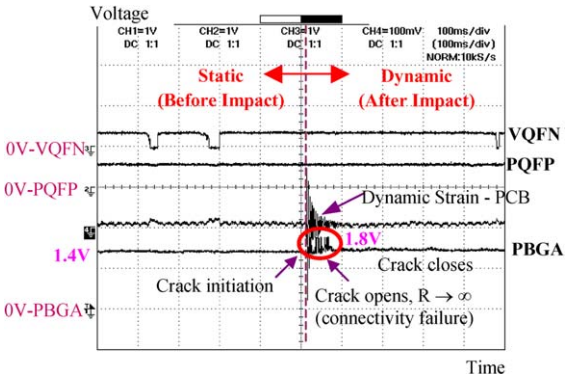

Fig. 7. Dynamic responses for Leg 3 (Pb-based on OSP) test board at 39th drop.

4.2. Drop impact test results

The summary of the impact test results is given in Table 1 for drops of 50 times conducted for every test board. The sample size is 6 for each test packages and legs. Failure sites for different test legs will be discussed before analyzing the results and failure trend obtained. In Leg 1 of the PBGA package with most failures occurred in less than 6 drops, five out of six failed units were detached away from the PCB. Possible failure sites of the PBGA solder joint are illustrated in Fig. 8. By examining the PCB where the PBGA detached from, solder ball to copper pad interface failure was found to be of majority. Clear solder joint cracks at the board side were found in the last remaining unit. Similar failure site was reported by Tee et al. [10] in their test for a fine-pitch BGA package of size 6.39 mm × 6.37 mm.

Table 1
Drop impact test results and summary

Test Leg	Frequency of failure	Number of drops to failure[a]
PBGA		
Leg 1[b]	6/6	1/50[c,f], 1/50[f], 1/50[f], 2/50[f], 6/50[f], 24/50[g]
Leg 2[b]	5/6[h]	15/50[d], 15/50, 19/50, 28/50, 47/50
Leg 3[b]	3/6[h]	12/50, 24/50, 40/50[e]
PQFP		
Leg 1	2/6[i]	44/50, 45/50
Leg 2	2/6[i]	16/50, 29/50
Leg 3	0/6	–
VQFN		
Leg 1	0/6	–
Leg 2	0/6	–
Leg 3	0/6	–

[a] A total of 50 drops were conducted.
[b] Leg 1 = Pb-free on ENIG, Leg 2 = Pb-free on OSP, Leg 3 = Pb-based on OSP.
[c] Illustrated by Fig. 5.
[d] Illustrated by Fig. 6.
[e] Illustrated by Fig. 7.
[f] PBGA units detached away from PCB after drop impact.
[g] Solder ball joint cracks found, component still intact on test board.
[h] Failure due to copper trace breakage.
[i] Failure not due to solder joint crack but component failure.

However, for the PBGA packages in Legs 2 and 3, PCB copper traces breakage and resin cracks were the contributing factor for connectivity failure (see Fig. 9). Lall et al. [8] also reported PCB resin cracks in the drop test of an 8 mm × 8 mm chip scale package. As for the PQFP packages where failures were also recorded, they were not due to solder joint crack but component failure instead. In Fig. 10, the lead fingers were found to break off from the mold compound due to the large impact force (inertial force) during drop. All the lead fingers are still intact properly to the test board. Some boards were tested beyond 50 drops. When dropped to 100 times, severe copper traces and PCB resin cracks were found. This revealed the underlying concern of PCB's reliability in drop impact which may provide misleading results for the study of solder interconnection strength. When drop test continued to 150 times, the VQFN solder joints still hold strongly onto the copper pads with no observed crack.

From the above observations, it can be seen that the type of surface finishes (i.e. ENIG versus OSP) does have a significant effect on the solder joint reliability between a package and the board. Interconnection between solder joints and board with Pb-free/ENIG configuration proved to be the weakest where failure had occurred in the intermetallic compound layer between the joint and copper pad. But for the Pb-free/OSP and Pb-based/OSP configurations, solder joint strength proved to be stronger due to the different intermetallic compound layer formed (to be elaborated more in the next section). With the stronger intermetallic adhesion strength, the failure site is being migrated to the copper traces and resin layers. This phenomenon has highlighted the importance of the quality of PCB in determining drop impact reliability. No solder joint failure was found in the Pb-free/OSP and Pb-based/OSP legs up to 50 drops. With the compliant gull-wing leads, the PQFP package outperforms the PBGA in drop impact reliability where the solder balls are more rigid. Being smallest in size and with the center pad holding the entire body firmly onto the PCB, the VQFN package proves to be most robust under drop test.

4.3. Failure modes and mechanism investigation of the PBGA solder joints

Under high strain rate test situations, brittle fracture is promoted through the suppression of plastic deformation [14]. Thus, drop test for soldered assemblies can cause brittle failure in the intermetallic compound

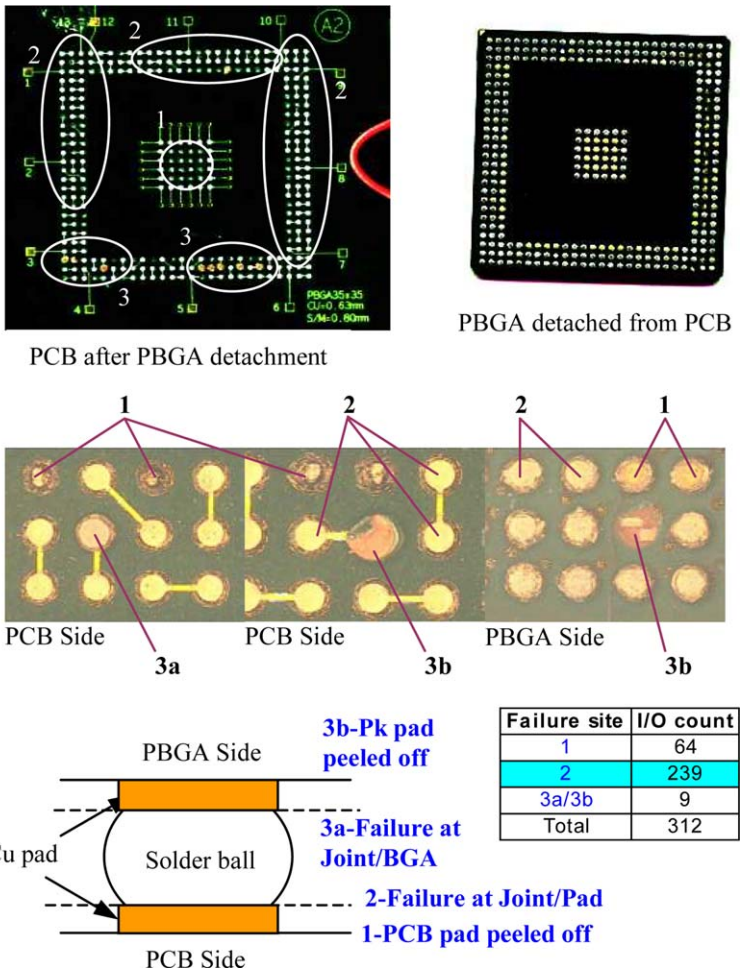

Fig. 8. Failure sites for the PBGA packages detached from the PCB after drop impact (Leg 1).

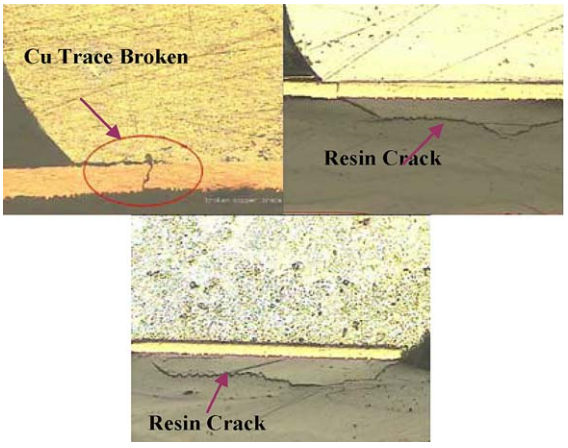

Fig. 9. Failure sites for the PBGA packages in Legs 2 and 3.

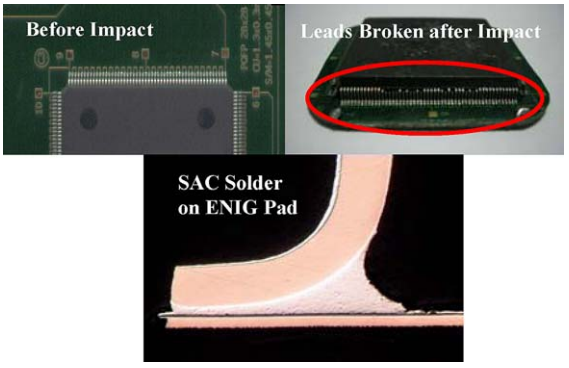

Fig. 10. Failure observations for the PQFP packages with good solder joints intact.

(IMC) layer instead of ductile failure in the solder. In the current drop test study, solder joint cracks were observed only in Leg 1 (Pb-free on ENIG) of the PBGA packages. And cracks were observed at the joint to PCB copper pad interface. For Pb-free and Pb-based solder

joints mounted on OSP coated copper pads, no joint interface failure was found. Hence different IMC layers formed with different surface finish can contribute to different failure modes. When Sn–Ag–Cu solder reflowed on the ENIG finish of copper pad, the gold plating (usually<1μm) dissolved rapidly into the solder and the nickel barrier layer forms a ternary intermetallic of Cu–Ni–Sn [13,15,16]. For Sn–Ag–Cu or Sn–Pb solder reflowed over an OSP copper pad, the OSP coating is evaporated and allows the interaction of the solder with copper to form a binary intermetallic of Cu_6Sn_5 [17,18]. The different layers of IMC formed in Leg 1 and Legs 2–3 are illustrated in Fig. 11. With ENIG process, phosphorous (P) present in the nickel plating bath generates

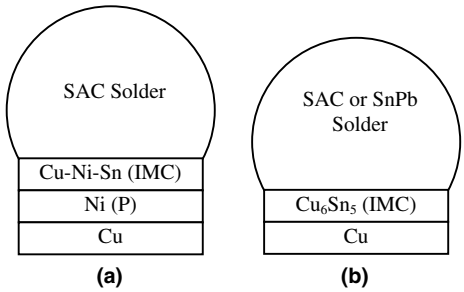

Fig. 11. Intermetallic compound layers formation for Legs 1–3. (a) ENIG pad finish (Leg 1) and (b) OSP pad finish (Legs 2 and 3).

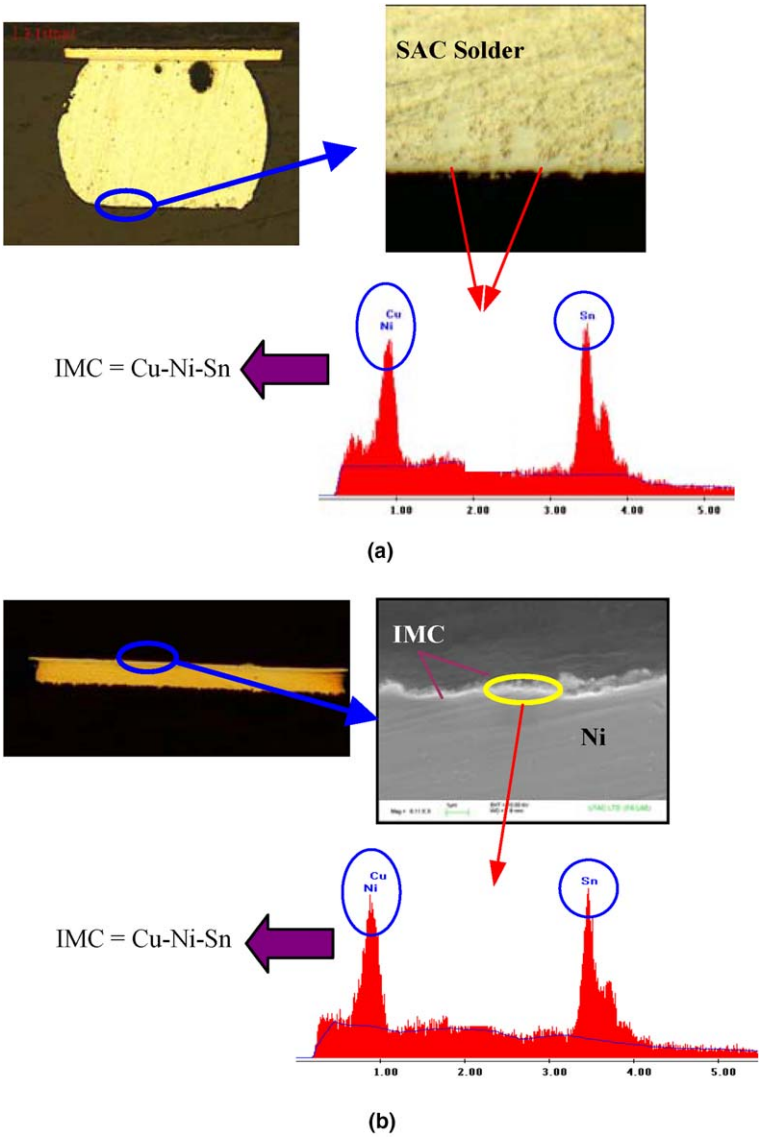

Fig. 12. Cross-sectioning interfaces of a PBGA detachment joint (Leg 1). (a) PBGA solder ball and (b) PCB copper pad.

a brittle Ni–P intermetallic compound segregating between the Cu–Ni–Sn intermetallic and the Ni(P) layer [19,20]. Mei et al. [20] showed that this Ni–P intermetallic is detrimental and leads to brittle interfacial fracture of BGAs solder joints.

Fig. 12 shows the cross-sectioning picture of a PBGA solder joint where the unit was detached away from the PCB after drop impact (Leg 1). Energy-dispersive X-ray spectrometry (EDX) analysis at the failure interfaces found that IMC of Cu–Ni–Sn were present at both the solder ball and copper pad interfaces. Fig. 13 shows another cross-sectioning picture of a Leg 1 PBGA solder joint where the unit remained intact on the PCB after drop impact. Referring to Fig. 13b, an IMC layer of Cu–Ni–Sn was present between the nickel plating and Pb-free solder ball. Solder joint crack was found to break through the interface of the solder to copper pad in Fig. 13a. A closer examination of the failure mode found that it actually cracked through the IMC layer. EDX showed evidence that IMC of Cu–Ni–Sn were found at both the solder and copper pad interfaces.

The intermetallic compound layers for SAC and Pb-based solders mounted onto an OSP copper pad (Legs 2 and 3) are showed in Fig. 14. From the EDX image, a binary IMC of Cu_6Sn_5 formation is evident. Based on the hardness test performed by Lee et al. [17], intermetallic of Cu–Ni–Sn (hardness = 6.9 GPa) has a higher hardness than Cu_6Sn_5 (hardness = 5.8 GPa), thus more prone to brittle fracture. Frear et al. [21] further determined that IMC of composition Ni_3Sn_4 is very brittle by hardness and fracture toughness tests. Chan et al. [22] also found that the brittle Ni_3Sn_4 IMC is the root cause for fracturing at the IMC layer. Studies by Mei et al. [20] and Bradley et al. [23] had revealed stronger adhesion strength of Cu_6Sn_5 intermetallic than Ni-Sn (due to the formation of Ni–P intermetallic layer). The above provides two explanations of the solder joints failure occurred in Leg 1 (Pb-free on ENIG) but not in Legs 2 and 3. Firstly, the joints have failed in the brittle Cu–Ni–Sn layer, whereas the Cu_6Sn_5 layer is more impact resistant. Secondly, interfacial cracks could initiate at the weak interface of Ni–P and Cu–Ni–Sn intermetallic and propagate through the Cu–Ni–Sn IMC layer. In Legs 2 and 3 where the solder ball is adhering to a larger surface of copper pad, the thin copper trace where it is experiencing much higher stress intensity due to drop impact failed instead. PCB resin cracks were found in all three test legs.

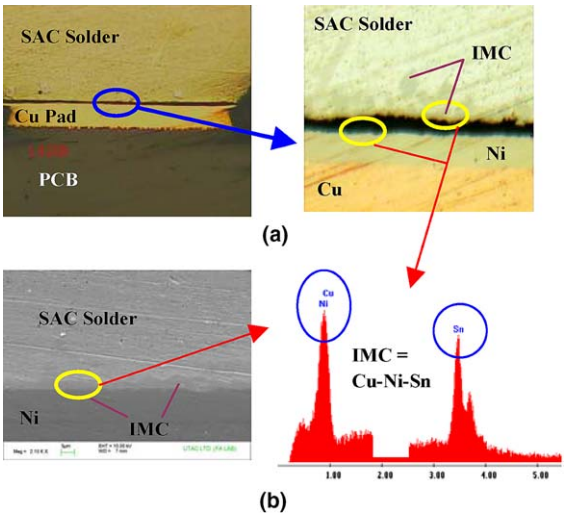

Fig. 13. Cross-sectioning and EDX of a failed solder joint—Pb-free on ENIG surface (Leg 1). (a) Cracked solder joint and (b) good solder joint.

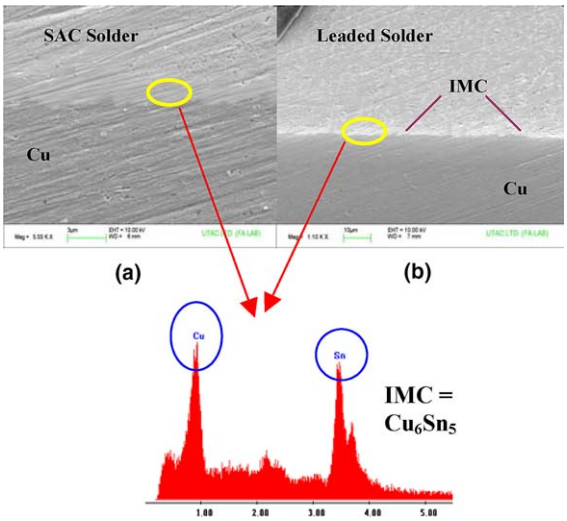

Fig. 14. Cross-sectioning and EDX of joints' interface in Legs 2 and 3 after drop impact (OSP surface). (a) SAC on OSP and (b) Pb-based on OSP.

Five out of six PBGA units in Leg 1 were detached away from the PCB after the impact test. The detachment could be due to combined effect of PCB bending and the large inertia force of the 35 mm × 35 mm package weight. A smaller BGA package (<15 mm × 15 mm) may not detach from the board, but cracks in the solder joints should be anticipated at the Cu–Ni–Sn intermetallic layers. Drop testing with smaller BGA components (e.g. 15 mm × 15 mm fine-pitch BGA) and the investigation of different solder compositions (such as SnAg) and other surface finishes (e.g. immersion silver or immersion tin) are considered for further investigation.

5. FE modeling and simulation for PBGA Pb-free solder joint

In this work, finite element (FE) modeling and simulation for PBGA assembly with Pb-free solder joint was

studied to investigate the stress–strain behavior of solder joint during drop impact loading. The quarter FE model as shown in Fig. 15 was used with the consideration of only the center PBGA component (marked as "B" in Fig. 1) based on the assumption that the effect of inertial force of one component on another one can be ignored due to low component mass and low stiffness of the interconnection. Symmetric boundary condition as shown in Fig. 15 along the cut boundary was used based on test conditions. The drop impact acceleration load as shown in Fig. 4a was applied onto the clamped boundary. In order to reduce simulation time without losing in accuracy, subcycling and mass scaling technique were implemented in the FE simulation. Many researchers [10,24] applied linear elastic material model for solder joint in drop simulation, which introduced more error on its stress strain behavior because plastic behavior will occur during high level dynamic loading. In this study, elastic material model and bilinear kinematic plastic model were considered for comparison. Table 2 lists the materials and their properties used in FE simulation for the PBGA assembly. Solving time of 15 ms was applied.

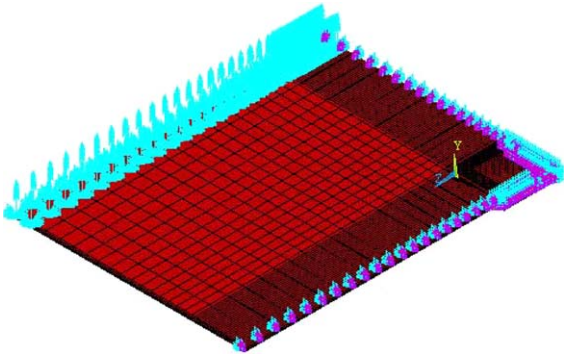

Fig. 15. Quarter FE model of the PBGA assembly with Pb-free solder joints.

Table 2
Material properties used in FE model

Materials	Young's modulus (MPa)	Poisson ratio	Density (10^{-9} Mg/mm^3)
Solder	41,730	0.35	7.5
Cu pad	155,170	0.34	8.9
FR4 PCB	x,z: 20,000; y: 9800	x,z: 0.28; y: 0.11	1.9
BT substrate	x,z: 26,000; y: 11,000	x,z: 0.39; y: 0.11	2.0
Die	131,000	0.278	2.33
Mold compound	16,000	0.24	1.97

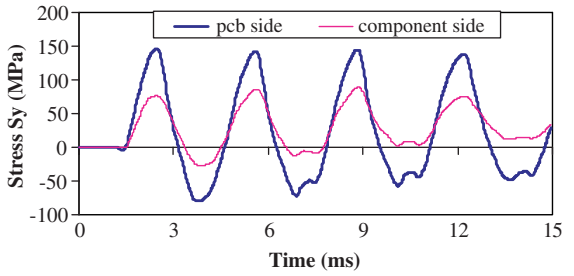

Fig. 16. Peel stress (Sy) variation of critical nodes on solder for both PCB and component sides.

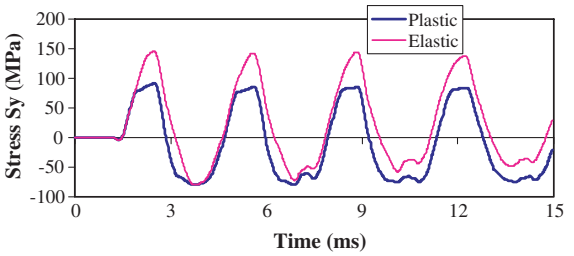

Fig. 17. Peel stress (Sy) variation of critical nodes on solder of PCB side from both elastic and plastic models.

From the simulation results, the peel stress in the direction of drop is dominant. Thus, this stress (termed as Sy) was selected as a failure parameter for comparison. Fig. 16 shows the stress history for critical nodes on solder/PCB interface and solder/component interface from the elastic model result. It can be seen that the stress on the PCB side is almost 2 times that on component side, which is consistent with the observation that failure is often occurring at the PCB/solder interface during drop impact loading. Fig. 17 shows the stress comparison between elastic and plastic models. It can be seen that the elastic model overestimates a stress of more than 50% compared to the elastic–plastic model. Therefore, plastic behavior must be considered for solder material subjected to drop impact dynamic load in order to obtain accurate results and for the evaluation of solder joint failure.

6. Conclusions

The drop impact reliability performance of the Pb-based and Pb-free solders IC packages has been assessed with surface finishes of ENIG and OSP. A new and simple dynamic resistance monitoring method demonstrated to be capable of capturing instantaneous drop impact failure and the explanation of interconnection failure process. The failure modes and mechanism of

the solder ball joints have been analyzed. The following conclusions can be drawn:

(i) The type of surface finishes (i.e. ENIG vs OSP) has a significant impact on the solder joint reliability between a package and the board.
(ii) Interconnection between solder ball joints and board of Sn–4Ag–0.5Cu/ENIG configuration showed to be weaker than the Sn–4Ag–0.5Cu/OSP and 36Pb–62Sn–2Ag/OSP configurations. The latter surface finish forms a much stronger joint integrity thus better survivability in drop impact test.
(iii) The Cu–Ni–Sn intermetallic compound forms a much weaker interface for drop impact resistant that Cu_6Sn_5 in a Pb-free solder joint interface.
(iv) The quality of PCB constituent materials such as copper traces, vias and resin etc are equally important in determining drop impact reliability performance.
(v) No failure observed in the PQFP package soldered joints implied that the gull-wing lead fingers are shock compliant and are able to absorb shock pulses resulted from drop impact.
(vi) Being smallest in size and with the center pad holding the entire body firmly onto the PCB, the VQFN package proves to be most robust under drop test.
(vii) FE simulation results show that a solder joint is prone to failure on the PCB side and the elastic model overestimates a stress level by more than 50%. Plastic behavior must be considered for solder material when subjected to drop impact loading.

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