Electronic Design

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11 Myths About SiP

The prevalence of system-in-package technology in a host of different applications has invariably led to myths about it. UTAC's Lee Smith dispels some of these fallacies.

System in package (SiP) is an invaluable tool for delivering compact silicon solutions. It allows different technologies to combine into a single package, reducing the bill of materials (BOM) of a system while increasing the reliability. It can also lower system design costs since more complex components are combined within a SiP.

There are many SiP implementations, so it's not surprising that a few myths about this technology may be floating around.

1. There's no industry agreement on the definition of system in package.

The definition of SiP varies so widely that the first chapter of TechSearch International's recent SiP report[1] includes a list of over 20 definitions, contributed by a range of SiP suppliers and users. To establish the basis for the report and forecasts, the chapter provides the following definition:

"System-in-Package is a functional system or subsystem assembled into a standard footprint package such as LGA, FBGA, QFN, or FO-WLP. It contains two or more dissimilar die, typically combined with other components such as passives, filters, MEMS, sensors, and/or antennas. The components are mounted together on a substrate to create a customized, highly integrated product for a given application. SiPs may utilize a combination of advanced packaging including bare die (wire bond or flip chip), wafer-level packages, pre-packaged ICs such as CSPs, stacked packages, stacked die, or any combination of these."

By this definition, multichip packages (MCP) and multichip modules (MCM) aren't considered a SiP, although various suppliers would disagree—this increases the challenge of analyzing and forecasting the SiP market. Many MCPs are combinations of devices that are like stacked-die chip-scale packages (CSPs), where flash and RAM are combined in a die stack supplied in high volumes. MCPs are also similar to MCM or modules, where the solution is a custom assembly format that's not a standard package platform, like a fine-pitch ball grid array (FBGA).

2. SiP competes with system on a chip (SoC).

They are more complementary than competitive. SoC has long been an effective strategy to integrate established IP blocks for high-volume applications that can absorb the significant complementary metal-oxide-semiconductor (CMOS) design and mask costs (which can exceed $300M) associated with a SoC.[2]

However, in today's system, semiconductor designers are looking for heterogenous integration solutions for SiP that have:

- Faster time to market.
- Lower design, non-recurring engineering (NRE) and development costs (rarely exceed $100k).
- Can integrate semiconductor devices (active and passive) that don't scale well in CMOS.

3. SiP requires known-good die (KGD).

KGD isn't required, but may be necessary. Many SiP products are assembled with die that rely on the same wafer probe test coverage as used in a single-chip package. KGD may be the right quality and reliability strategy for a complex SiP that requires a costly substrate or component bill of materials (BOM). For high-volume SiP assembly, die is supplied in wafer form. Thus, defining the best probe flow (which could include burn-in or voltage screening) is critical in developing your KGD strategy and supply chain.[3]

4. Heterogeneous integration (HI) will replace SiP.

HI should be seen as the big-picture view for semiconductor technology road-mapping beyond Moore's Law. In contrast, SiP is the integration of various semiconductor devices within a given package platform. The International Technology Roadmap for Semiconductors (ITRS) is transitioning from a concentration of roadmaps for semiconductor fabrication scaling to outlining the roadmap challenges and requirements

for heterogeneous integration technologies.[4]

5. SiP requires a printed-circuit-board (PCB) laminate substrate.

Due to strong demand for passive integration (primarily capacitors and inductors) in power-management applications, leadframe-based SiPs are seeing strong growth. Prismark Partners forecasts that 3.5 billion leadframe-based power SiP will ship by 2021.[5] Leadframes provide low cost and high thermal conductivity, making them a strong SiP platform for lower I/O and higher power requirements.

Laminate-based SiPs in land-grid-array (LGA) and ball-grid-array (BGA) configurations (primarily assembled in strip formats) serve the widest range of SiP applications; laminates support higher-density interconnection requirements with wide design flexibility, due to the wide range of laminate fabrication technologies. Wirebond, flip chip (FC), stacked die, embedded die or passives, and high-density SMT are all readily enabled through laminate substrates.

Emerging high wiring density applications are shrinking conductor line and space widths below 12 microns with roadmaps below 5 microns. This is driving adoption and development of new SiP platforms such as FanOut wafer, panel-level CSP, and the use of silicon or glass-based interposers with high-aspect-ratio through vias.

6. SiP is a planar 2D assembly.

With the growth in die stacking, package-in-package assembly, package-on-package (PoP) stacking, and embedded die technologies, 3D package architectures are providing size and performance advantages over 2D planar assemblies. 3D SiP solutions offers the following performance advantages:

- 3D SiP not only provides package footprint reduction on a printed-circuit-board assembly (PCBA), it also enables an increase in semiconductor content-to-package ratio through 3D integration technologies. The increased semiconductor content includes 3D integration of both active and passive devices.
- Reductions in package footprint can improve package warpage control, PCBA assembly, as well as second-level solder-joint reliability.
- Improved electrical performance through short vertical interconnects that can reduce circuit delays.
- Enable electromagnetic-interference (EMI)/radio-frequency-interference (RFI) shield isolation between semiconductor devices for radio-frequency and digital integration requirements.

7. The SiP architecture, process technologies, and materials are more critical than the supply-chain business model.

The supply-chain business model can make or break the success of a SiP in the market. A SiP solution can have 100 components in the electronic bill of materials (eBOM), but if one component isn't available due to delivery or quality problems, it stalls SiP manufacturing.

SiP solutions require advanced microelectronic package assembly and test capabilities. With the strong trend to outsource manufacturing services in the semiconductor and electronics industry over the past 50 years, outsourced semiconductor assembly and test (OSAT) providers have been the leaders in developing and scaling up of advanced packaging technologies.

The OSAT business model as a contract package assembly test provider to their semiconductor customers has been based on the consignment of wafers. OSAT supply chains have focused on equipment, circuit carriers (leadframe, substrate, etc.), and materials requirements. The growth in SiP has been driven by smartphone applications over the past 15 years, which has required OSAT supply chains to develop sources for electronic components. However, OSATs procure a very small percent of electronic components (estimated at 1%).

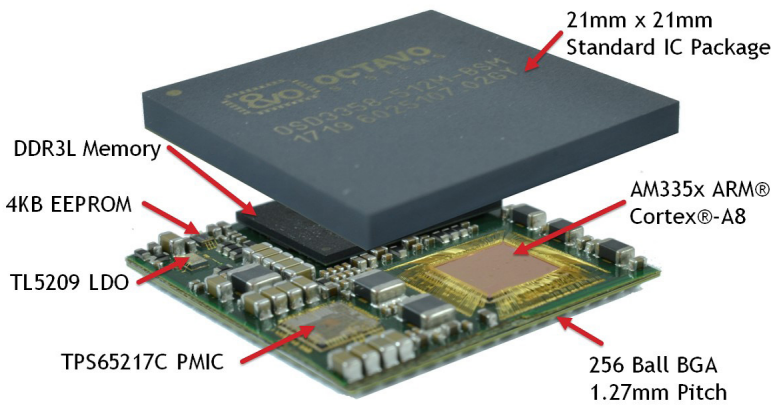
In a difficult business environment for electronic components (due to escalating component prices and lead times), demanding a full turnkey business model could adversely impact a SiP's cost and time to market. Thus, SiP customers should team with OSAT suppliers in defining the optimum business model:

- *Consignment model:* Where the SiP customer procures and consigns the eBOM, which is managed by the OSAT provider.
- *Pass-through-pricing (PTP) model:* Where the SiP customer has contractual agreements for key components and establishes supply terms for pass through pricing for the OSAT to procure at the contractual terms. This is common when custom components are specified or customers have a limited source of components qualified.
- *Full turnkey model:* Where the SiP customer requires the OSAT provider to source and manage the eBOM.
- *Combination business model:* Where certain key components may be consigned or managed, as PTP and standard components need to be procured by the OSAT or contract manufacturer.

8. There are no new business models in the semiconductor industry.

With the record number and value of mergers and acquisitions in the semiconductor industry over the past three years,[6] industry analysts and trade editors have focused on the trends and consequences of strong market consolidation. Due to the high cost of entry into the slowing and highly competitive semiconductor industry, analysts speculate that the industry is nearly closed to new entries and new business models. There's speculation that the following business models will continue to dominate the industry going forward:

- *Integrated device manufacturers (IDMs):* Own and maintain semiconductor fabrication factories.
- *Fabless device suppliers:* Focus on design and IP, and rely on contract manufacturers to fabricate, assemble, and test



Shown are the semiconductors used in Octavo Systems' OSD335x-SM BGA SiP-based product.

their devices.

• *Foundry suppliers:* Provide contract semiconductor fabrication services to fabless and IDM suppliers.

However, SiP technology is enabling a new semiconductor industry business model to emerge—an electronic systems integration provider. An electronic systems integration provider relies on advanced substrate and microelectronic assembly technologies to design a system or subsystem solution by integrating various semiconductor devices, delivered in a SiP format. Octavo Systems is an example of this emerging business model.[7] The *figure* illustrates the semiconductors (bare and packaged ICs) used in Octavo's OSD335x-SM product delivered in a 21- × 21-mm, 256-ball BGA SiP solution.

The Octavo Systems website features information on the trends and solutions available through SiP as a systems integration platform. To understand the potential of this new business model, companies will need to explore the product innovations and new services emerging for Internet of Things (IoT) applications. New IoT applications are being developed across all industries, including banking, manufacturing, retail, healthcare, transportation, utilities, and government. The revenue potential for IoT-based products and services is forecasted to approach $270 billion by 2020.[8]

9. SiP is only used for miniaturization.

Miniaturization is a key advantage of SiP, but performance and system optimization are equally important in today's thrust for higher levels of integration. Many original equipment manufacturer (OEM) system suppliers have added engineers with strong microelectronic packaging experience to help them better define system architectures and new supply chains to expand their use of SiP and module solutions. These suppliers have support from electrical, thermal, and mechanical design/simulation teams who have the tools needed for system performance or reliability optimization. Semiconductor and OSAT suppliers have also expanded their engineering and design/simulation teams to apply a broader range of advanced packaging technologies to develop new SiP solutions.

In addition, semiconductor foundries and electronic manufacturing service (EMS) providers have added skills and capabilities to provide highly integrated solutions like SiP or modules. The use of SiP is quickly expanding in lower-performance applications like IoT connectivity and high-performance systems like 5G networks.

10. SiP is limited to a sole-source supply chain.

Multi-sourcing is a common requirement for high-volume applications. A wide range of OSATs have advanced package assembly capabilities and offer broad SiP services. If multi-sourcing is required for high volume or assurance of supply requirements, it's recommended to develop supply-chain strategies to address the following:

• Copy exact or copy equivalent requirements. Copy equivalent allows suppliers to apply their qualified material sets, as well as enable alternate sources for passive components.

• Multi-source qualification.

• Market-share agreements for sharing of volumes and maintaining capable sources of supply.

• Open sharing of design or manufacturing cost and quality improvements.

• End-of-life product management.

11. SiP is only economical for low-performance applications.

SiP solutions aren't limited to low-performance requirements and are in production across a diverse range of applications. Computing, gaming, communications, and networking require high performance for challenging electrical, thermal, and mechanical requirements with long product lives. Along with 3D SiP architectures, SiP solutions can enable miniaturization and semiconductor integration to enhance system performance by increasing bandwidth, lowering power, enabling increased functionality, and integrating mixed semiconductor process nodes—in smaller product footprints with increased time to market.[9]

Lee Smith is Vice President of Advanced Packaging Products at UTAC. He has broad expertise in microelectronics and strong network within the electronics industry. As a thought leader in advanced and 3D packaging, Lee is recognized for driving the technology and market development for package on package (PoP). Lee also possesses

a strong passion for growing business and helping customers succeed in bringing products to the market.

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