Development Approach & Process Optimization for Sidewall WLCSP Protection

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Wafer Level Chip Scale Package (WLCSP) has become the fastest growing IC package type serving a broad range of applications due to its small / thin form factor, strong supply chain and low overall cost. While there are many devices and end applications for WLCSP technology, the mobile phone market is recognized as the major growth driver and is driving WLCSP technologies to handle smaller and thinner die with finer ball pitches. As a result WLCSP is forecasted to grow over 15% annually to exceed 42 billion units shipped in 2019 [1].

WLCSP has many benefits; however the industry is demanding solutions to address two major quality and reliability challenges. First, as applications demand smaller and thinner die in WLCSP, the risk of die handling defects rise due to the absence of die side wall protection such as an encapsulation layer. The second major challenge for WLCSP is thermal and mechanical stresses that impact a product's board level reliability. The risks for solder joint failures increase as WLCSP ball diameter and ball pitches shrink due to die size reduction and higher functional integration which increases ball count densities.

Handling defects such as, die corner stress, chipping and or die cracks can cause functional failures which may happen during the WLCSP processing or arise over the electronic product's life due to environment temperature or mechanic use stresses. WLCSP handling defects can occur at any step across the device process flow from WLCSP back end processes of dicing through tape and reel packing to the final surface mount of the WLCSP device on the product printed circuit board assembly (PCBA). The cost impacts of a function failure, is highest if it occurs in the field, next highest if occurs or is detected in the final PCBA (whether PCBA rework is feasible or not). To prevent or sort out WLCSP fabrication and handling defects, expensive equipment has been implemented for wafer dicing

(especially for devices with fragile low K inner layer dielectrics) and to perform post saw inspection to detect and contain die and side wall defects. WLCSP assembly houses have deployed expensive back side wafer film lamination, laser scribe / dice and 5 side inspection equipment to reduce die back and side wall stresses and detect chipping and die cracks. SMT pick and place handling defects of WLCSP devices increase in level with small and thin die. Due to the high density of PCBAs that contain one or more WLCSP devices it is hard to characterize and eliminate SMT handling defects as die continue to get smaller and thinner. As a result new more mechanically robust WLCSP structures are required to reduce the risks through the final printed circuit board and higher level electronics assembly processes.

To address handling issues, the industry has been seeking die sidewall protection solutions to encapsulate fragile silicon die [2]. Figure 1, illustrates the 5 side encapsulated WLCSP reported by STATS ChipPAC at ECTC in 2014.

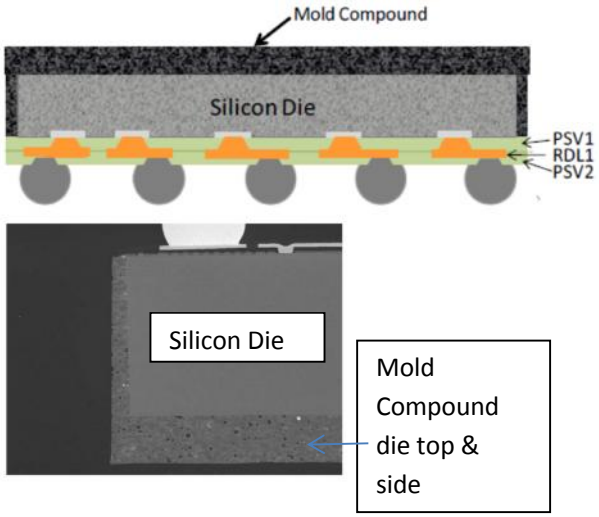

Figure 1. Encapsulated WLCSP structure and Cross section (BGAs up view)

To address board level solder joint reliability issues the industry has been seeking solutions ranging from Fujitus's Super CSP structure shown in Figure 2 [3] to wafer applied encapsulation materials to coat the fragile solder ball to UBM interface as shown in Figure 3 [4].

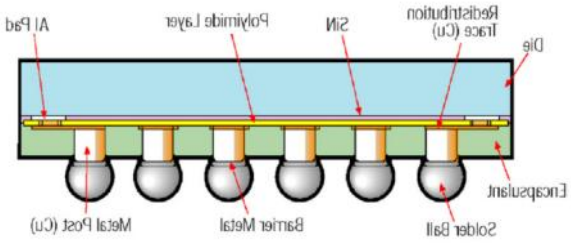

Figure 2. Super CSP structure

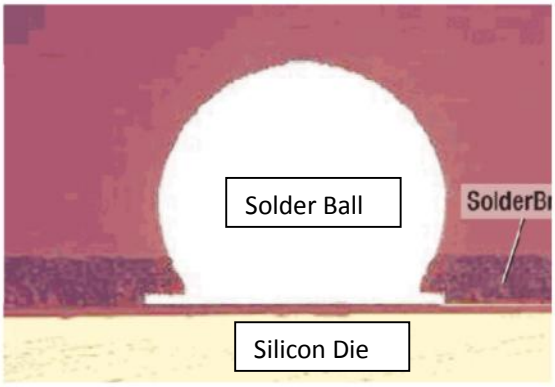

Figure 3. Solder Brace coated WLCSP

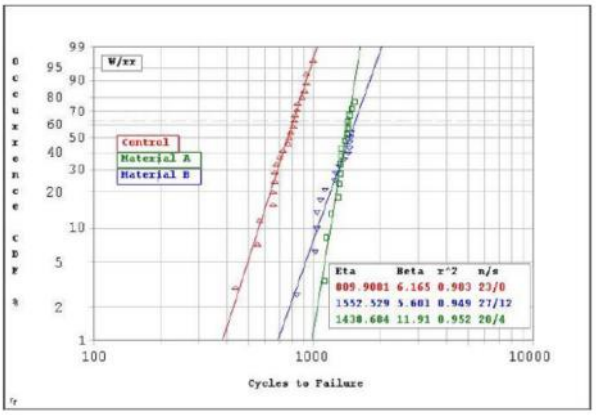

Figure 4. Weibull plot of control die and die coated with solder supporting materials A (50µm thick coating) and B (70µm).

The Super CSP structure did find production WLCSP applications but the combination of plated copper posts and wafer mold encapsulation processes have limited adoption due to high manufacturing costs.. The solder brace material did see industry collaboration studies for board level reliability [5] showing improvements in temperature cycle (-40 to 125 C) life as shown in Figure 4, however the material has not been reported in production applications or studies. In addition these structures lack a die side wall protection layer so would still be subject to die handling defect challenges.

To address both of the major challenges limiting WLCSP quality and reliability performance UTAC is developing a sidewall protection solution using wafer-molding of the active die side following ball attach. This presentation will: Illustrate UTAC's WLCSP side wall protection structures, Figure 5 shows structure with full side wall mold protection and back side film.

Summarize development approaches and key process optimizations to scale this technology into high volume manufacturing.

Process limitations and challenges will also be presented with risk mitigation approaches studied and applied.

WLCSP Sidewall protection development based on wafer back end processing with no wafer re-constitution or additional redistribution layers required.

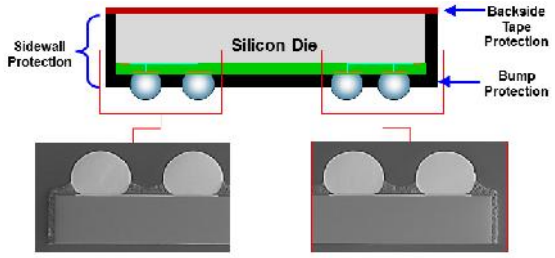

Figure 5: UTAC WLCSP full sidewall protection Structure with back side film

Key Features this Structure Provides :

1. Mechanical support of solder balls – improves temp. cycle life of 2nd level BGA interconnects
2. Protects die sidewalls –reduces risk of sidewall chipping, die crack or crack propagation
3. Backside film protection (which is an optional structure)

Wafer molding optimized for good moldability with different mold compound types and thickness as shown in Figure 6.

Figure 6. Molded full wafer and die BGAs side mold compound support view

References

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