Multichip Integrated Copper Clip Package Technology, Supports High Current DC-DC Converter Applications

Michael-HyungMook-Choi, Kyaw Ko Lwin and Lee Smith; UTAC Group

COPPER CLIP INTERCONNECT plays a critical role in DC-DC converter power MOSFET package technology to address: lower total device resistance RDS(on), higher power density and high frequency switching requirements. [RDS(on) stands for "drain-source on resistance," or the total resistance between the drain and source in a Metal Oxide Field Effect Transistor, or MOSFET] [1]. The copper clips replace traditional wire bond interconnects for low voltage MOSFETs by providing lower interconnect resistance and inductance than multiple wire bonds. Copper clip interconnects have been widely used in discrete MOSFET packaging from the late 1990's and now package assembly technology has advanced to enable multichip integrated solutions like DrMOS (driver IC and 2 MOSFETs). This copper clip based package integration solution provides key advantages of small foot print and lower parasitic inductance.

DrMOS (Stands for Driver + MOSFET)

The concept of DrMOS was suggested by Intel over a decade ago [2], as CPU power requirements were increasing with every process generation. Intel suggested that voltage regulators (VR) that support a CPU need to operate at very low voltages (~1V) and very high currents (100+A) with fast dynamic response to meet transient voltage requirements. To meet these new VR requirements, power semiconductor suppliers needed to solve 3 technology challenges to meet CPU requirements in PC desktop and server markets:

1. Increase power density of power stages.
2. Increase switching frequency to meet faster dynamic response requirements.
3. Provide these performance advancements in a scalable low cost, high volume technology platform.

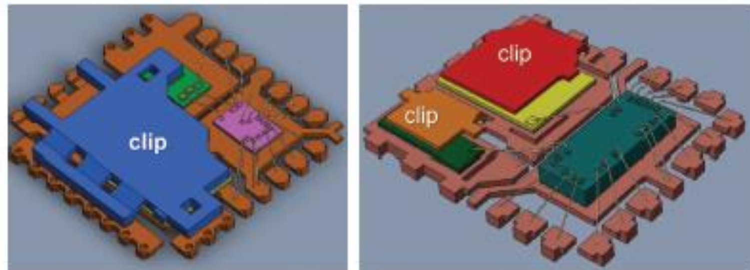

Figure 1. Side by side clip configuration example, 2 MOSFETs are soldered on 2 separate die attach paddles (left drawing has 1 copper clip (shaded blue) and right drawing has 2 copper clips (shaded orange and red).

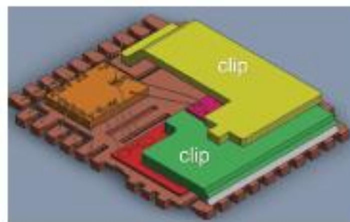

Figure 2. Stack clip configuration example which has 2 MOSFETs and 2 clips (bottom green and top yellow) are soldered on same die attach paddle.

These DrMOS requirements have driven technology advances in VR building blocks including the development of a low cost, scalable multichip package platform. For the server market requirements, the package technology must enable integration of 2 different size MOSFETs and their CMOS driver IC, into a small surface mountable platform. Since PC market growth had stalled, UTAC chose to focus on the DrMOS package requirements for the more challenging server market. For servers, DrMOS packages need to enable both side by side and stacked MOSFET combinations which provide tool up and assembly challenges for copper clip interconnects. UTAC has been qualified in high volume production of QFN with side by side clip configuration. Also with stack clip configuration packages. See Figure 1 (side by side clip configuration) and Figure 2 (stacked clip configuration).

DrMOS Application Markets:

DrMOS products are used in Synchronous Buck regulators which can be found in various applications:

- Desktop and Server VR buck-converter
- Single Phase and Multiphase point of load (POL) in fixed telecom power supplies
- CPU/GPU voltage regulation in desktop and notebook Graphics Cards, DRAM DDR Memory, Graphics Memory etc.
- High Power Density Voltage Regulator Modules (VRM)

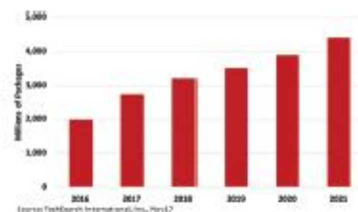

Figure 3. Power QFN with Copper clip market.

Figure 3, provides a forecast for the world-wide Power QFN market with Copper clip interconnects [3]. The market is forecasted to grow at a 17% CAGR from 2016 to over 4 billion packages by 2021. Further market research indicates, the main growth applications, require multichip integration requiring more complex copper clip interconnect structures.

Potential New Applications of Integrated Copper Clip Technology

Gallium nitride (GaN) is a wide band-gap semiconductor material with high heat capacity and thermal conductivity widely used in high brightness LED applications. GaN's electrical properties of high breakdown voltage and electron mobility, make it an ideal material for high power applications. [4] Power semiconductor suppliers are developing GaN MOSFETs as a next generation power switching device to replace standard silicon MOSFETs especially for higher switching DC-DC converters.

One emerging GaN MOSFET applications is for wireless charging, to enable the efficient transfer of power to devices without the use of wires. Here an independent industry group called the Alliance for Wireless Power (A4WP) was formed to develop and maintain standards for a new form of wireless power [5]. The A4WP standard differs from other wireless charging approaches by using a relatively high frequency of 6.78 MHz. Power semiconductor supplies are considering GaN based FETs integrated with a driver IC and copper clip interconnects as a candidate multichip package solution.

Emerging DrMOS 6 x 5mm QFN Electrical Spec Comparison for High Current GPU Graphics Card

To date, the most popular DrMOS Power QFN package size has been 5 x 5mm. However, emerging high-performance GPUs and bitcoin ASIC processors need higher current DC-DC converters which benefit from a larger body size DrMOS 6 x 5mm QFN in the printed circuit board assembly (PCBA) to effectively handle the higher currents.

	Body Size [mm]	Packages	Area	
Driver IC	3 x 3	8	72	mm2
MOSFET	6 X 5	18	540	mm2
	TOTAL PCB AREA		612	mm2

Figure 4a. GIGABYTE-GeForce-GTX-1080 VGA Card with Discrete MOSFET and driver IC.

	Body Size [mm]	Packages	Area	
Driver IC	0	0	0	mm2
DrMOS	6 X 5	12	360	mm2
	TOTAL PCB AREA		360	mm2

Figure 4b. GeForce-GTX-1080 EVGA card with 6 X 5 DrMOS MOSFETs (forums.evga.com).

Figure 4a and 4b shows examples of Graphic Cards in the market with 2 different DC-DC converter solutions. Figure 4a is Geforce-GTX-1080 VGA card PCBA with discrete packaged MOSFETs and driver ICs and Figure 4b is Geforce-GTX-1080 EVGA Card with DrMOS in 6 x 5mm power QFN packages.

The discrete solution in Figure 4a has 8 Driver ICs packaged in 3 x 3mm QFN mounted within the red box area. Then within the yellow boxed area there are18 MOSFETs packaged in 6 x 5mm Power QFN. This discrete solution consumes a total PCB area of 612 sq. mm for the 26 packages.

Figure 4b shows the integrated DC-DC converter solution with 12 DrMOS in 6 X 5mm Power QFN, requiring only 360 sq. mm which is about 40% smaller PCB area than the discrete solution of Fig4a requiring 14 less packages as the Driver IC is integrated in the DrMOS.

To demonstrate the electrical performance benefits of DrMOS in 6 x 5mm Power QFN, comparison of conventional wire bonding to copper clip interconnects

is illustrated in the following figures and electrical parameter simulations table. For simulation purposes, a low side MOSFET die is fixed at 2.9 x 4.0mm which is close to the max die size of 6 x 5mm Power QFN MOSFET. Copper wire is 2mil (50μm diameter) and copper clip thickness is 10mil (250μm).

Figure 5a shows MOSFET die (pink perimeter) is attached on top of the lead frame (gray) and 22 copper wire bonds are required to connect the MOSFET die to package leads on the left side. The figure on the right is the top side view to better show MOSFET die pads and copper wire interconnects. The MOSFET die has 6 separate source pads (marked as S), the 2 small pads on the left side of the die require 3 wires each and 4 large pads require 4 wires each for total source copper wire count of 22 wires.

Figure 5b shows that higher copper wire bond interconnect density is required to achieve the electrical performance for a MOSFET designed for higher switching speeds. Here 9 source pads (marked S) are required for faster switching, each pad requires 3 wires for a total of 27 wires. One can envision how 1 copper clip is a more efficient solution providing improved cost and performance vs 27 wire bonds.

Figure 6 shows the copper clip interconnect structure for the standard MOSFET shown in Figure 5a. Here the MOSFET die is fully covered by the interconnect of a copper clip. The soldered connection of copper clip to the MOSFET die provides reduced interconnect contact resistance. The copper clip structure provides a significant reduction for package resistance and inductance compared with the copper wire bond shown in Figure 5a.

Table 1 provides the electrical parameter simulation comparison between copper wire bond interconnection shown in Figure 5a and 5b, vs copper clip interconnection shown in Figure 6. Resistance values of Figure 5a using copper wire bond interconnects is 0.46m ohm and the faster switching design Figure 5b is 0.37m ohm which is around 20% lower due to use of 5 more source wires. However, with a copper clip interconnect, the resistance is 0.047m ohm which is about 90% lower resistance than copper wire bond due to the higher thickness of the copper clip and larger areas of contact to the MOSFET die and Power QFN leads.

The inductance values of the interconnect technology are simulated at 0.084 nH and 0.076nH with wire bonding and 0.044nH with copper clip technology, nearly a 50% reduction in package inductance.

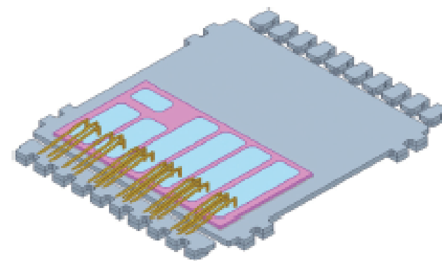
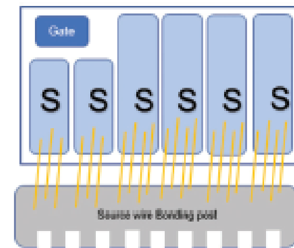

Figure 5a. Copper wire interconnect and bonding diagram views.

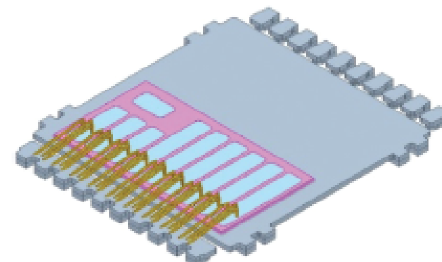
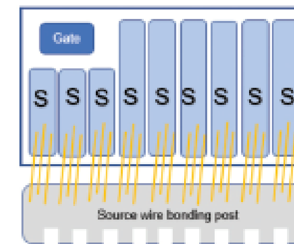

Figure 5b. Copper wire interconnect and bonding diagram view of fast switching MOSFET.

UTAC Copper Clip Based Power QFN Offerings

As shown in Table 2, UTAC is in production with various Power QFN sizes with copper clip interconnects. Both gold (Au) and gold / palladium / copper (AuPdCu) wires are used for Driver IC interconnect based on the customer's requirements. These products support different copper clip configurations including:

- Stack clip structure (MOSFETs and copper clips are vertically stacked together)

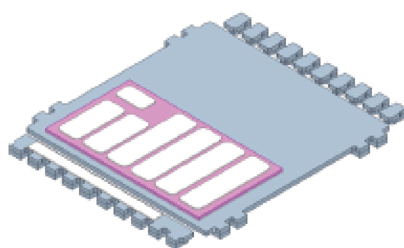
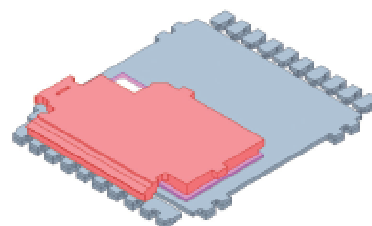
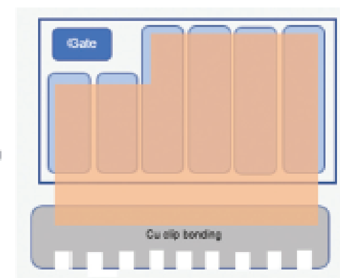

Figure 6. Copper clip MOSFET die on lead frame and copper clip attachment and clip bonding diagram.

- Side by side copper clip structure (MOSFETs are attached on 2 different leadframe die attach pads (DAP) with separate copper clips attached. This configuration isolates the low side MOSFET and high side MOSFET on 2 separate DAPs.
- Single clip structure (MOSFET and copper clip on 1 DAP).

For more information about UTAC please visit www.utacgroup.com. ◆

References

[1] 2017 May 5, Scott Thornton https://www.microcontrollertips.com/mosfets-what-is-rdson-faq

[2] 2004 Nov Intel DrMOS rev 1.0 release https://www.intel.com/assets/pdf/refmanual/drmos.pdf

[3] TechSearch International, Advanced Packaging Update. Market and Technology Trends, Volume 3 Nov. 2017

[4] Wikipedia; Gallium nitride https://en.wikipedia.org/wiki/Gallium_nitride

[5] A4WP Wireless Charging https://www.electronics-notes.com/articles/equipment-items-gadgets/wireless-battery-charging/a4wp-wireless-charging.php

Material	Dimension	Resistance (mΩ)	Inductance (nH)	Remarks
Copper Wire (5a)	50 µm x 22 wires	0.46	0.084	Parasitic value includes wires and leads
Copper Wire (5b)	50 µm x 27 wires	0.37 (20% lower)	0.076 (10% lower)	Parasitic value includes wires and leads
Copper Clip (6)	0.254 mm thick	0.045 (90% lower)	0.044 (48% lower)	Parasitic value includes solder, clip and leads

Table 1. Electrical parameter simulation comparison.

UTAC: Integrated Cu Clip Products							
Body Size	6x4	5x5	5x6	6x5	5x4	6x5	5x5
Lead	36	31	41	12	18	16	32
IC	1	1	1	1	1	1	1
MOSFETS	2	2	2	2	2	2	1
# of Clip	2	2	2	2	2	2	1
config	Stack	side by side	stack	stack	stack	side by side	single
Wire	Au 1.3	Au 1.3	AuPdCu 1.0	AuPdCu 1.0	AuPdCu 1.0	AuPdCu 1.0	Au 1.3

Table 2. UTAC copper clip product body size and configuration examples.

ONE COMPONENT
SILVER FILLED EPOXY
NASA Low Outgassing Approved
EP3HTS-LO
ELECTRICALLY CONDUCTIVE
Volume resistivity: <0.001 ohm-cm
THERMALLY CONDUCTIVE
12-15 BTU•in/(ft²•hr•°F)
HIGH STRENGTH PROFILE
Tensile strength: 4,000-6,000 psi
FAST CURING
45-50 minutes at 250°F
MASTERBOND®
ADHESIVES | SEALANTS | COATINGS
+1.201.343.8983 • main@masterbond.com
www.masterbond.com