

GUIDELINES FOR PRINTED CIRCUIT BOARD ASSEMBLY (PCBA) OF UTAC GROUP'S GRID ARRAY PACKAGE (GQFN) AND ITS BOARD LEVEL RELIABILITY

Kyaw Ko Lwin*, Daniel Ting Lee Teh, Carolyn Epino Tubillo, Jun Dimaano,
Ang Choon Ghee, Nathapong Suthiwongsunthorn, Saravuth Sirinorakul
United Test and Assembly Center Ltd
Singapore

*Email: kolwin_kyaw@utacgroup.com

ABSTRACT

Over the past 17 years, leadless lead frame packages have been continuous advancements in density, thickness, reliability and performance. The vast majority of leadless lead frame packages have a single row of perimeter pads limiting their application to low pin count devices, typically below 100. This paper will introduce advancements UTAC has made in leadless lead frame assembly, materials and process technologies which enable QFN packages to address challenging application and device requirements through improved reliability and higher I/O densities. UTAC's new generation of leadframe package design called Grid Array QFN (GQFN) allows traces to be routed through etching process and providing higher I/O, reduction of package size up to 40%~60%, shorter wire length compared to QFN. Flip chip, stack die, multi-chip module and SiP options are also possible. GQFN package is also feasible for solder ball drop or solder coat option on terminal which offers alternative to ball grid array package. Unlike solder mask based lead insulation process, GQFN's insulation mold process eliminates complex multi-step process flow which raises cost and manufacturing challenges.

GQFN's Printed Circuit Board Assembly (PCBA) guidelines will be discussed in this paper. It will cover PCB design, Land Pattern, Component placement, Stencil design, Reflow Profiles (Eutectic and Pb-free) as well as Rework Process. Mobile applications require new package technologies to retain solder joint integrity over more stringent temperature cycle stress and drop shock use cases (board level reliability). GQFN's board level reliability will be assessed following PCBA guidelines. GQFN design reduces the package size by 60% compared to QFN, the increased die-to-package ratio poses concerns on board-level reliability (BLR) as the silicon is known to be a major source of coefficient of thermal expansion (CTE) mismatch between package and PCB which add more impact on solder joints. Demanding

handheld use cases are driving mechanical drop shock resistance targets up, with customers requiring data up to 1,000 drop cycles. GQFN package has good board level reliability results meeting the test requirement according to the IPC/JEDEC standards.

Key words: GQFN, BLR, PCB assembly, Insulation mold

INTRODUCTION

Leadless leadframe packages have been introduced to semiconductor industries more than a decade ago and there have been continuous advancements in package's structure, reliability and performance. Quad Flat No lead (QFN) packaging is widely accepted in the industry due to low cost, small footprint, its ability to implement die attach paddle for better heat dissipation and good electrical performance. However, most of the QFN packages have a single row of perimeter pads limiting their application to low pin count devices, typically below 100 I/Os. UTAC's Grid Array QFN (GQFN) packaging is driven by the need to miniaturize the package, simplify the assembly process and provide a lower overall cost by using advancements in leadless lead frame assembly, materials and process technologies. GQFN routing technology enables multi-row or full grid array pad densities and smaller form factor.

GQFN process flow is shown in Figure 1 and grid array configuration is available with a routable lead frame-based technology. The metal leadframe is fabricated with partially etched and selectively plated before delivered to the package assembly line. The selective plating is for featuring package terminal pads and die paddle after etch back process. The assembly process starts with front of line (FOL) process where die attach and wire bond are performed. Although, illustration in Figure 1 is for wirebond option, GQFN packaging supports flip-chip, stacked die and passive integration options as well.

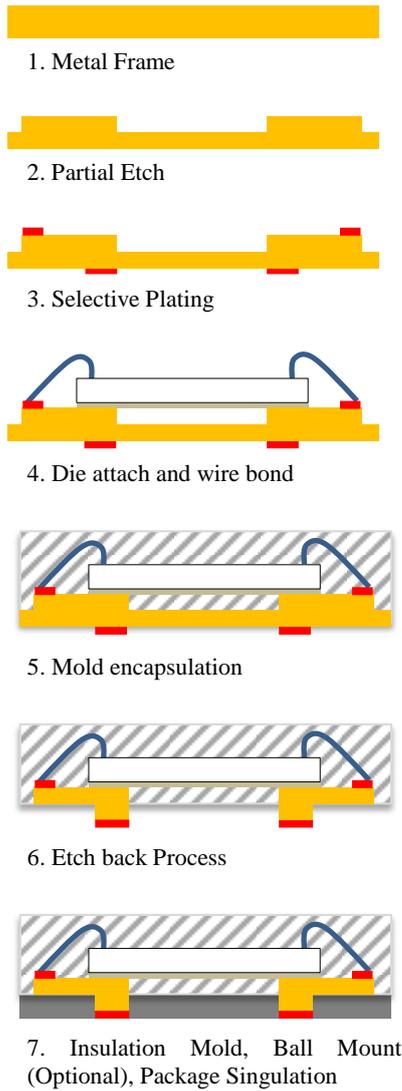


Figure 1: GQFN packaging process flow

After FOL process, end of line (EOL) process continues with upper mold encapsulation. Subsequently, two key processes of GQFN are followed; etch back of the leadframe to fabricate the routings and isolate the terminal pads and an insulation mold process to complete the package encapsulation. GQFN bottom terminations can be completed with optional printed solder coat or ball drop for higher standoff before saw singulation. Figure 2 shows GQFN's flat terminals and solder balls option.

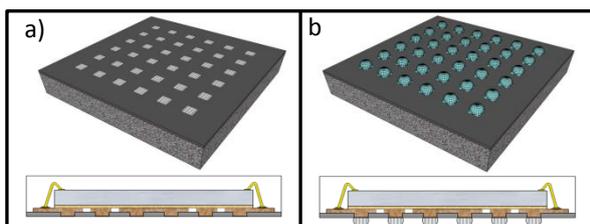


Figure 2: Package structure and cross section of GQFN, (a) flat terminals, (b) solder balls.

Solder mask based lead insulation processes requires complex multi-step process flow which raises cost and manufacturing challenges. It limits adoption of area array QFN technology. As shown in Figure 3 GQFN's insulation mold process eliminates complex solder mask process [1]. On the other hand, GQFN's Insulation Mold also poses assembly challenges and several factors including process and material had to be optimized during the development of insulation mold process capability.

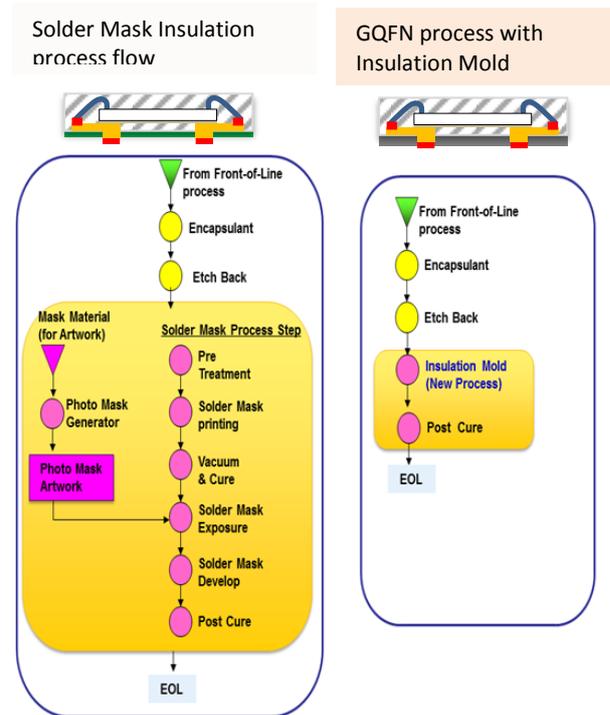


Figure 3: Solder mask insulation and mold insulation process

Insulation Mold

GQFN Insulation Mold process poses risk in term of mold filling ability because of tight clearance in bottom half etch leadframe. UTAC practices Mold flow simulation to conduct mold flow behavior analysis for process, design and materials optimization. Figure 4 illustrates Mold flow simulation for insulation mold process showing well balanced melt front. Mold flow simulation is to study the melt front imbalance and flow resistance at small gap or irregular shaped area of the package. Packing pressure, transfer profile, material and leadframe design were optimized and potential risk was mitigated.

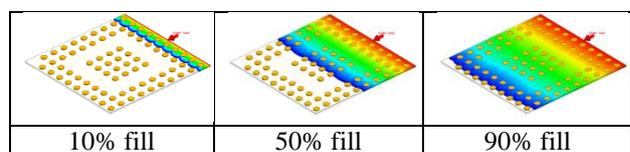


Figure 4: Insulation mold flow simulation

Package characterization

GQFN package advancement in routing technology enables full grid array solution with excellent thermal, electrical and mechanical performance. With routable traces and array I/Os, it is feasible to convert organic substrate base package to GQFN for better reliability and lower cost. Figure 5 illustrates ball grid array (FBGA) comparing with GQFN.

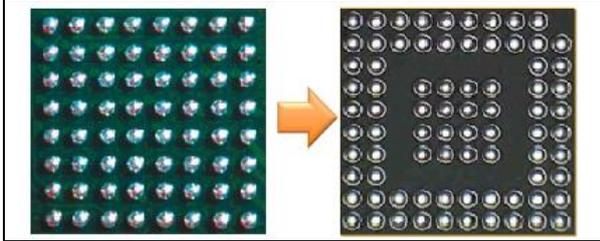


Figure 5: Ball layout of FBGA 5x5mm and GQFN 5x5mm (right)

Thermal performance

GQFN packaging can deploy die attach paddle option with thermal balls for efficient heat dissipation, enabling excellent thermal performance and high power usage. It has been reported that GQFN exhibits better thermal characteristics compared to two layers FBGA package [2]. The Computational Fluid Dynamics (CFD) simulation study were performed with both substrate FBGA and GQFN packages having identical power dissipation, die size, die thickness and test environment except differences in package structure such as two layers substrate with vias for FBGA model and routable leadframe for GQFN model. UTAC's thermal simulation set-up is in accordance with JEDEC recommendation (JESD51) [3] [4] [5]. Figure 6 demonstrates thermal test set up for still air environment.

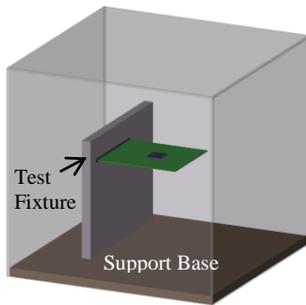


Figure 6: JEDEC Still Air Chamber set up

Figure 7 shows temperature distribution plots from Flotherm CFD simulation. GQFN's Die junction temperature is 3.85 °C lower and Theta JA is 12.5% improved. Table 1 is the overall thermal resistance data for both packages and GQFN has superior thermal capability in all aspects.

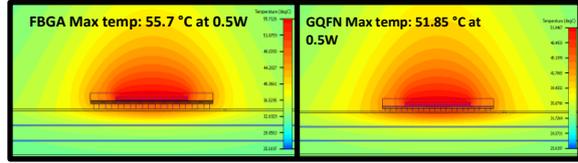


Figure 7: Temperature distribution of FBGA 5x5mm and GQFN 5x5mm (with 4x4 arrays of thermal balls at Still Air Test condition on 2S2P thermal board)

Table 1: Full thermal characterization result

Thermal resistance	Air flow (m/s)	Package Type		% improvement
		FBGA 5x5mm (°C/W)	GQFN 5x5mm (°C/W)	
Theta JA	0	61.4	53.7	12.5%
Theta JMA (moving air)	1	52.6	46.2	12.2%
	2	51.0	44.7	12.4%
	3	49.9	43.7	12.4%
Theta JB	0	32.0	24.1	24.7%
Theta JC	0	11.7	10.7	8.5%

Electrical performance

GQFN's flexible interconnectivity between chip and board allows shorter electrical paths and supporting high frequency application. Scattering parameters (S-parameters) of both packages were compared for high frequency application using Advance Design System (ADS) simulation tool [2]. UTAC follows JEP126 standard for electrical model analysis of IC package [6]. Figure 8 shows 3D models for electrical simulation without showing mold compound.

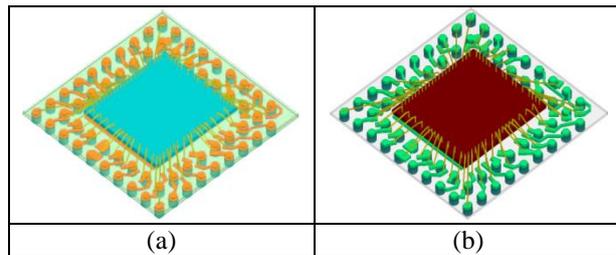


Figure 8: 3D models, (a) FBGA 5x5mm, (b) GQFN 5x5mm

A frequency sweep from DC to 30GHz was run on the same net (longest electrical path) of both GQFN and FBGA packages. Assumed -15dB is Return Loss requirement to have good signal performance, GQFN package will survive up to 3.9GHz that is 1GHz higher than FBGA counterpart that is limited to 2.85GHz as shown in Figure 9.

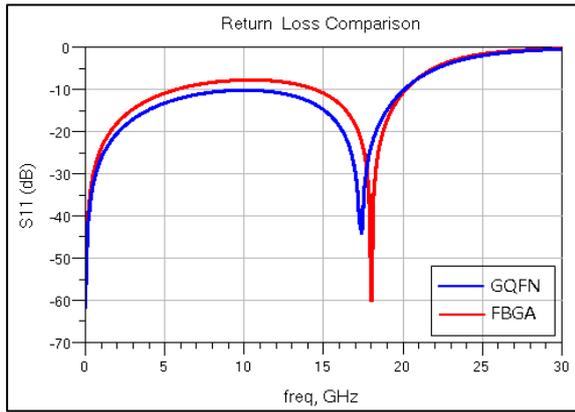


Figure 9: S-parameter (Return Loss) plot for FBGA 5x5mm and GQFN 5x5mm

GQFN packaging offers smaller form factor and package bottom termination by engaging routing technology with multi-row or full grid array pad layout. Figure 10 illustrates package footprint reduction between Quad Flat Package (QFP), Quad Flat No lead (QFN) package and GQFN package. The same number of I/Os are maintained in all three packages.

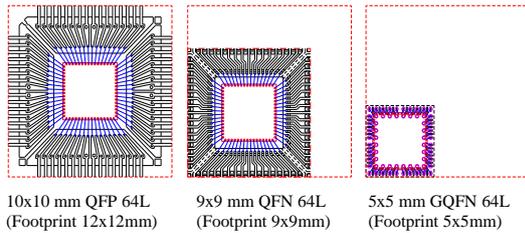


Figure 10: Package footprint comparison between QFP, QFN and GQFN

The advantage of routable leadframe is the flexibility to organize critical electrical paths for optimum parasitic values. Figure 11 illustrates capacitance and inductance values comparing the shortest nets among three package types for low frequency applications. [1]

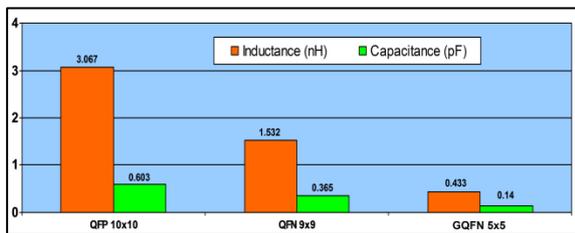


Figure 11: Package's parasitic values comparison of QFP, QFN and GQFN with same I/Os.

GQFN's PCB Assembly guidelines

UTAC provides PCBA application note as a general guideline. SMT process development intended for a specific application or requirement is recommended. Prior to SMT of component, PCB shall meet the solderability requirements as per ANSI/J-STD-003 [7] and be flat to within 0.1 mm per linear cm. Thermal vias should be implemented on the PCB thermal pad to boost thermal performance. The number thermal vias depends on the package thermal requirement determined by thermal simulation or actual test. Filled or plugged vias should be considered for better thermal performance.

The PCB land pattern should match the GQFN terminal and exposed pad dimensions indicated in the package outline drawings. The PCB terminal should be approximately a 1:1 ratio with the package lead. Variation in PCB pad size is possible depends on requirement. Figure 12 shows GQFN 5x5mm package outline with thermal balls.

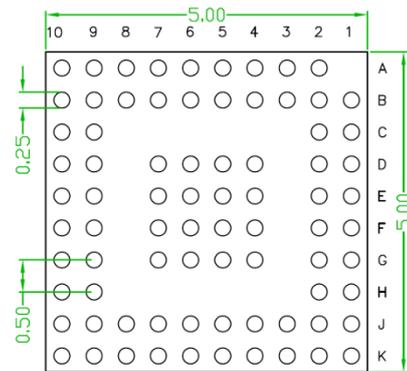


Figure 12: Package outline drawing showing bottom view

Stainless steel stencils with thickness of 0.075mm – 0.127mm (3 –5 mils) are recommended for solder paste application. Stencil aperture sizes should be 1:1 with pad size. However certain parts may require reduced aperture size. Stencil thickness and aperture openings should be adjusted for optimal solder volume.

“No clean” paste is recommended for assembling the GQFN to the PCB, due to its low standoff and small pad openings. For fine terminal pitch, such as 0.40mm, type 4 solder paste is recommended.

GQFN packages can be very small with fine terminal pitches and typically require 0.050 mm package placement tolerance and low placement pressure to prevent paste smearing or squeezing out of the solder joint.

The package can be attached to the PCB by convection mass reflow techniques as part of standard

SMT process. Thermal profiling of the reflow machine is required for each product design. Reflow profile should follow the solder paste supplier's recommendation. In case of eutectic solder, the reflow temperature shall not exceed 240°C with time above liquidus temperature (183°C) of 45 seconds. For Pb-free solder, the reflow temperature shall not exceed 260°C with time above liquidus temperature (217°C) of 45 seconds.

GQFN rework processes are very similar to or simplification of ball grid array package's rework processes. The rework steps can be summarized as below.

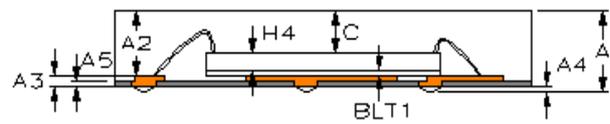
- Board preheat to 120°C to avoid warpage
- Solder reflows of component to be removed
- Vacuum removal of component
- Cleaning and preparation of PCB lands
- Screening of fresh solder paste
- Placement and reflow of new component
- Inspection of solder joints

Several automated rework systems are available which can address the previous steps with high precision in a single machine.

Board Level Thermal Cycling Test Reliability

GQFN routable capability enables small package form factor with tight Die to package clearance, reduction of package size up to 60% compared to QFN package. Increasing die to package ratio poses thermal cycling on board reliability concern as silicon is well-known to be the major source of coefficient of thermal expansion (CTE) mismatch between package and PCB. Higher CTE mismatch will induce higher solder joint stress forcing the joint to fail earlier. UTAC performed GQFN board level reliability following PCBA guidelines discussed above for mounting of daisy chain units on test board.

GQFN 7x7mm with 162 pre-coat solder balls is used for thermal cycling on board (TCoB) reliability test. The ball pitch is 0.5mm and overall package thickness is 0.75mm including solder standoff. 4.2x4.2mm dummy die is attached at the package center and daisy chain connection is formed by lead to lead bonding with gold wires. Figure 13 illustrates GQFN package structure. SAC305 is used for pre-coat solder with diameter 0.25mm and height 0.1mm. PCB is designed such that it will form integrated daisy chain connection with package as per IPC-9701A recommendation [8]. 4-layer PCB is fabricated with high Tg FR-4 and 1mm thick. PCB dimension is 200x150mm and 12 daisy chain units were mounted on one side. Air chamber was used for accelerated temperature cycling range at -40°C to 125°C with 15min dwell and 15min ramp, 1 cycle per hour as in Figure 14.



PACKAGE THICKNESS (A)	0.75mm
MOLD CAP THICKNESS (A2)	0.55mm
LEADFRAME THICKNESS (A3)	0.101mm
DIE THICKNESS (H4)	0.203mm
BLT1	0.025mm
SOLDER BALL THICKNESS(A4)	0.100mm
POST MOLD THICKNESS(A5)	0.050mm
CLEARANCE BETWEEN TOP SURFACE OF DIE & MOLD CAP (C)	0.322mm

Figure 13: GQFN Package Structure

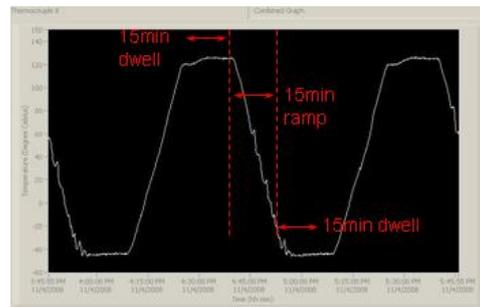


Figure 14: TCoB temperature cycle from -40°C to 125°C

Event detector and data logger were used for in-situ electrical resistance monitoring and a failure criterion is 20% nominal resistance increase for five consecutive readings. Total 48 units were tested for TCoB and all units survived up to 1,100 cycles without failure. Figure 14 is two parameter Weibull plot and characteristic life is 1,780 cycles. Characteristic life is prediction for 63.2% of failures. The failure analysis was performed by characterizing cross section of solder joint with scanning electron microscopy (SEM). The common failure was bulk solder fracture near package side at package to solder interface as shown in Figure 15. Although the die size is big with die-to-package ratio of 60%, GQFN 7x7mm exhibits good TCoB performance.

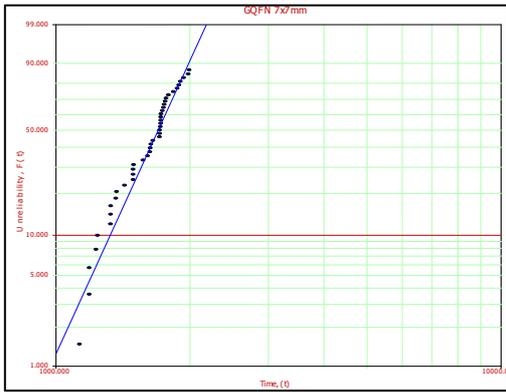


Figure 14: Weibull plot for TCoB characteristic life

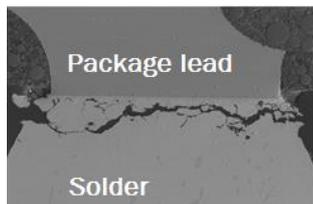


Figure 15: Bulk solder fracture

Board Level Drop Test

The Board Level Drop Test is intended to evaluate and compare dropped performance of surface mount electronic components for handheld devices in an accelerated test environment. The excessive flexure of a circuit board causes product failure in the test environment [9]. To conduct the board level drop test, GQFN 7x7mm daisy chain packages were SMT on 132x77x1.0mm 8-layers board which was designed to form an integrated daisy-chain with packages as per JESD22-B111. The board is mounted on drop table with components faced down as shown in Figure 16. The drop height was calibrated such that the free-fall dropping of the board using a drop table generated 1500 g's deceleration with half-sine pulse duration of 0.5 millisecond corresponds to JESD22-B111 Condition B.

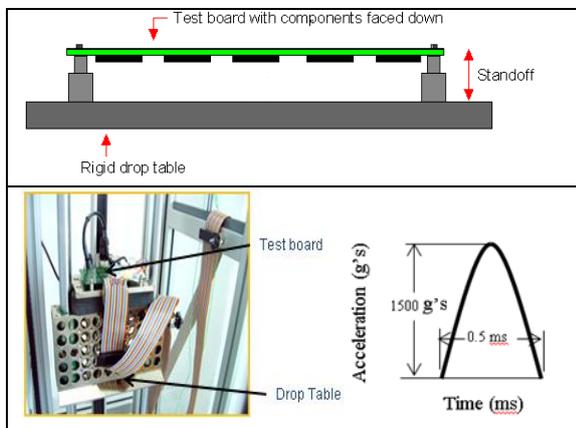


Figure 16: Drop test setup

Thirty daisy chain units were tested for board level drop performance as per JEDEC standard and all units pass 30 drops requirement. The Weibull characteristic life is 420 cycles as shown in Figure 16.

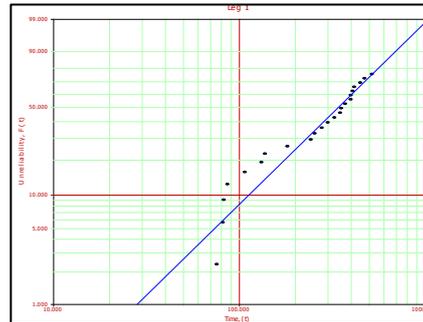
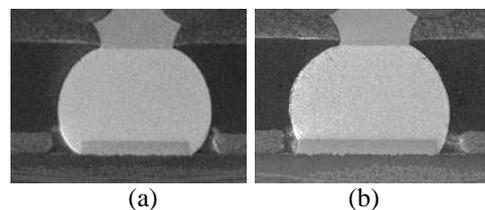


Figure 16: Weibull plot for drop test. PCB pad size impact on BLR

UTAC suggests PCB terminal pad size to be approximately a 1:1 ratio with the package lead. However, some applications may require variation of the PCB pad sizes. Figure 17 illustrates section view of solder joint where GQFN package is mounted on non-solder mask defined (NSMD) PCB. 10 mils lead-free solder ball was attached to 150um package pad. Figure 17a showing a good barrel shape solder joint with solder wetting on both sides of PCB pad where the diameter is 25% larger than package pad. In Figure 17b, PCB pad is 65% larger than package pad and the solder joint wetting is on only one side of the PCB pad.



**Figure 17: Section view of solder joint
(a) PCB pad is 25% larger than package terminal
(b) PCB pad is 65% larger than package terminal**

The black data point in Figure 18 Weibull plot represents case (a) solder joint and the characteristic life is 8% longer than case (b).

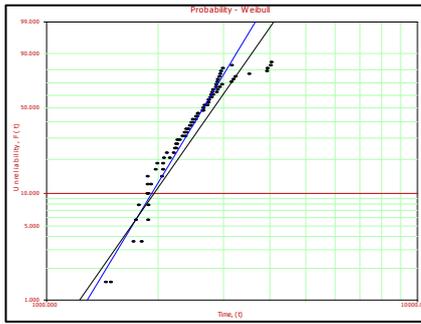


Figure 18: Weibull plot for TCoB characteristic life comparing different PCB pad sizes

In this study, both cases met the requirement of minimum 1,000 TCoB cycles. With small foot print and moderate Die to package ratio, there is low risk of early TCoB failure and big tolerance in PCB pad size is still acceptable.

CONCLUSIONS

GQFN packaging applies standard assembly process and eliminates complex process required by substrate based insulation process. GQFN's routable leads and full grid array option provide a cost advantage per I/O when compared to QFN and two-layer laminate package options. The integrated grid array solution exhibits excellent thermal and electrical characteristics with capability to handle high power and high-frequency requirements. GQFN's PCB assembly guideline covered from PCB land pattern design to re-work process was discussed. Several GQFN packages following the SMT guidelines were qualified for second level reliability. BLR qualification of GQFN 7x7mm with Die to package ratio of 60% was discussed in the paper. The package shows robust board level characteristics for both TCoB and Drop Test. The study of different PCB pad sizes suggested that a good barrel shape solder joint contributes to better board level reliability.

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