Development and Package Characterization of Advance Leadless Lead-frame Package

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Abstract

This paper addresses the development of advance leadless lead-frame package which was driven by the increasing demand for higher I/O density, smaller footprint and better performance packages at a lower cost. Grid Array Quad-Flat No-Leads (GQFN) package is a new leadless lead-frame based technology that offers an ideal solution to the industry's demand and requirement. The advantages of this package includes limitless design flexibility that allows interconnect trace routing to enable multi-row or full array pad configurations leading to higher I/O feasibility which rivals various laminates packages such as BGA or LGA. GQFN design has smaller package form factor with reduction of package size up to 60%, shorter wire length, allows flip chip, multi-chip module, and passive integration. This new innovative design was enabled with UTAC's advancement in process and materials technology within the industry. Key processes and challenges will be discussed in the paper.

This paper reveals the package structure and investigation of performance and reliability of GQFN package by presenting comprehensive simulation and experiment work done. Simulations are executed to fully characterize the thermal, electrical and mechanical performance of GQFN. With the direct thermal path of die paddle underneath the die, superior thermal performance is achievable. GQFN's routable leads enable shorter electrical path as well as lower internal impedance which enable gigahertz (GHz) capability. GQFN showed robust second level reliability by passing both stringent temperature cycles on board (TCoB) and drop test. Mold flow simulation was also conducted to check any unbalanced melt front in molding process to ensure no internal voiding occurs due to complicated lead frame routing and thin gap design. In this paper, detailed analyses of the package's performance are discussed in depth.

Key words: GQFN, Insulation mold, Thermal, Electrical, Simulation, Board Level Reliability

Introduction

With recent trend and the race to increase functionality in smaller size consumer electronic devices such as smart phones, electronic wearables, and laptops there is a demand for higher pin count packages while maintaining quality, miniature size, low cost and peak performance. Leadless leadframe package such as Quad Flat No Lead (QFN) is a popular cost-effective and high performance packaging solution in semiconductor industry. [1] However, there is a limitation in design flexibility and low I/O or pin counts due to the restrictive peripheral array of lead frame design. Switching to laminates based packages solution such as BGA and LGA is needed for higher design flexibility as these packages are able to accommodate several layers of circuit routing within substrate which comes at a higher price. Low cost solution is a more preferred choice hence advance leadless packages with higher I/O density are developed. The competition to develop smaller footprints and high functionality packages at a low cost has been an ongoing challenge for outsourced semiconductor assembly and test services (OSATs) companies. Achieving a good balance between cost, quality, reliability and high functionally is the utmost importance in any new package development. To address the need for higher density I/O packages, United Test and Assembly Center (UTAC) and other OSATs have developed numerous types of low-cost multiple row QFN that offered higher I/O density with various acronyms such as Dual Row QFN (DR-QFN) [2] as shown in Fig. 1, Thermal Leadless Array (TLA) package [3] shown in Fig. 2, Thin Array Plastic Package (TAPP) [4], Multi Row(MR) QFN [5], Advanced QFN (aQFN) [6], Micro Lead frame package (MLF) [7] and Hi-density lead frame array (HLA) [1] shown in Fig. 3.

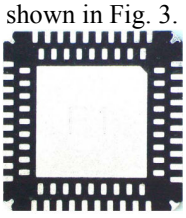


Figure 1: Dual Row QFN 7x7mm 76L package

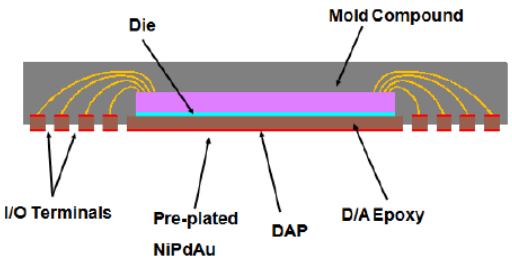


Figure 2: Thermal Leadless Array (TLA)

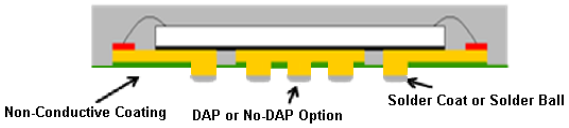


Figure 3: Hi-density Lead frame Array (HLA)

These packages have superior electrical and thermal performances as they have smaller body, shorter interconnect and lead frame based. HLA package has the highest design flexibility and capabilities to provide high I/O density with lead frame routing using etch back and solder mask or non-conductive coating lead insulation process technology. However supply chain, cost and manufacturability obstacles are limiting the adoption and ramp up of these solutions. [8] To overcome these obstacles, alternative methodologies which utilized the standard assembly processes have been developed at UTAC to serve the demand of highest I/O density with lead frame trace routing technology. With the advancement in process and materials technology as well as using insulation mold process, it is possible to produce scaled up high-volume manufacturing for multi-row or full grid array with high-density lead routing packages.

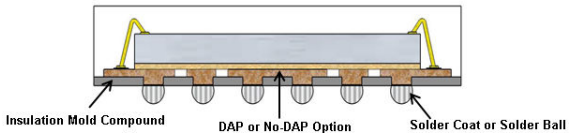


Figure 4: Grid Array QFN (GQFN)

UTAC's new generation of high density lead frame package design is called Grid Array QFN (GQFN) shown in Fig. 4 above. GQFN a revolutionary package which allows traces to be routed through etching process and providing higher I/O density, reduction of package size up to 60% and shorter wire length compared to QFN. The routable technology enables design flexibility and fully customizable lead frame design which provides a brilliant solution to existing lead frame design restriction. With the design flexibility, the package is able to support stacked die, multi-chip module (MCM), passive integration, System in Package (SiP) using flip chip and/or wirebond interconnection. [9] Besides that, GQFN package is also feasible for solder ball drop or solder coat option on terminals which offers an alternative to laminates based BGA / LGA packages.

Process flow of GQFN

Figure 5 below illustrates the process flow of GQFN package. The metal frame is partially etched and selectively plated on both side of the lead frame surfaces depending on customer's design. Subsequently, the lead frame is delivered to the package assembly line for IC assembly where die attach and wirebond or flip chip takes place. Once front of line (FOL) processes are completed the package top is encapsulated with mold compound. After the first mold top encapsulation, the lead frame undergoes etch-back process to complete the trace routing and isolate pre-plated leads to enable multi-row or full array I/O pad configurations. The package encapsulation is then completed with insulation mold process. Finally, printed solder coats or ball drop for higher stand-offs can be performed before package saw singulation.

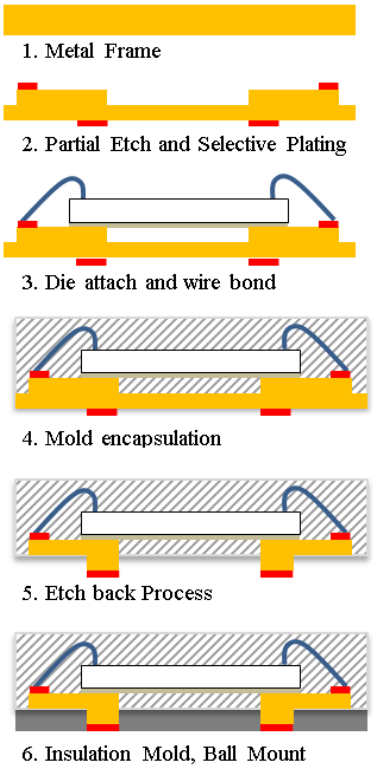


Figure 5: Process flow of GQFN package

GQFN package includes the usage of two different mold compounds material where top mold is a standard QFN mold compound while the bottom insulation mold compound has enhanced material properties to fill the tight clearance at the bottom half etched leads gap area. Similar to GQFN package, HLA package uses double half-etch lead frame process technology however this package uses solder mask-based lead insulation process instead of insulation mold. Unlike solder mask based lead insulation process, GQFN's insulation mold process eliminates complex multi-step process flow which raises cost and manufacturing challenges and limits the adoption and scale up of the HLA solution as shown in Figure 6.

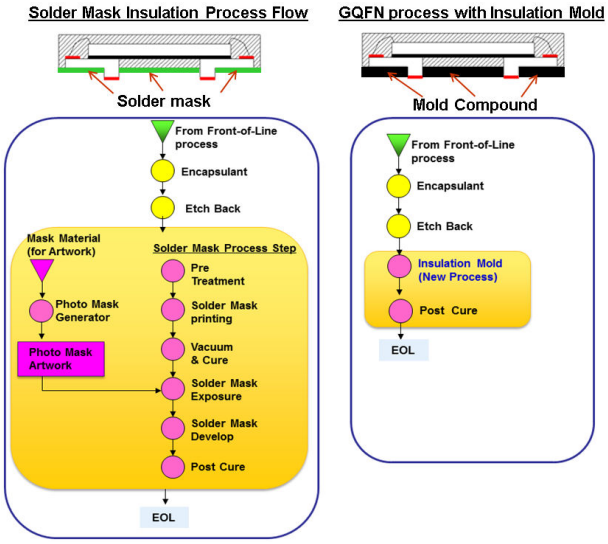


Figure 6: Solder mask insulation and mold insulation process

Manufacturing Challenges

The entire process may seem straight forward but the double molding process has proved to be a challenge and UTAC has devoted the time and effort to evaluate options to optimize the insulation mold process and assembly. To overcome this, several process and material factors had to be optimized to deliver high volume capable assembly process. Some of the factors include: a) Mold tooling design; b) Film assist molding; c) Process parameters, transfer profile and pressure; and d) Mold material properties and fine filler technology. [8] GQFN design uses two different mold compounds and supports extra thin mold cap thickness. Warpage is a known issue as chemical shrinkage and CTE mismatch will induce deformation on the entire strip during the mold curing process. Warpage trend analysis using finite element analysis (FEA) software ANSYS was conducted on generic xGQFN package (extra thin mold cap thickness GQFN) to select the most favorable standard epoxy mold compound (EMC) on the top side to reduce warpage. In post mold cure process warpage simulation and trend analysis, stress free temperature is assumed at 185°C and room temperature at 25°C.

Table 1: Epoxy Mold Compound Material Properties

Item	EMC A	EMC B	EMC C
Tg (°C)	180	130	130
CTE 1 (ppm/°C)	12	7	9
CTE 2 (ppm/°C)	48	30	36
Equivalent CTE (ppm/°C)	13.1	14.9	18.3
Note: Equivalent CTE = [(185-Tg) x CTE2 + (Tg-25) x CTE] / (185-25)			

The warpage is developed towards a crying shape. Figure 7 shows that higher equivalent CTE mold compound is needed on the top side mold of extra thin GQFN to control the warpage as the insulation mold (bottom mold) CTE is relatively high. Analysis results were validated with actual panel and strip warpage which showed good trend correlation. Bigger die size will also increase the warpage as it has effect on the overall CTE mismatch within the system.

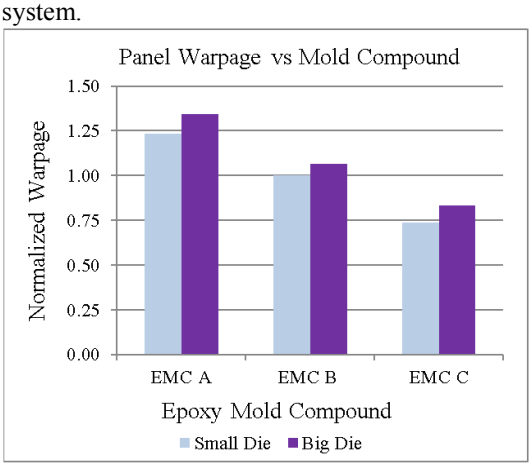
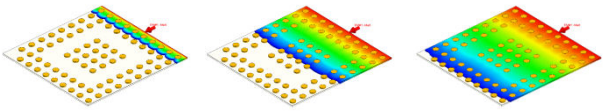


Figure 7: Warpage trend for different EMC

The clearance of the insulation mold is tight hence insulation mold flow process poses risk of mold filling ability and incomplete filling. Besides that, lead frame customization and design flexibility leads to irregular shaped I/O pads which result in imbalance mold flow and voids entrapment. Internally, mold flow simulation can be conducted to predict the melt front merging location of the insulation mold. UTAC has the capability to perform mold flow simulation at package and panel level. The purpose of mold flow simulation is to study the melt front imbalance and flow resistance at small gap or irregular shaped area of the package. Applying the experimental method to optimize flow process is time consuming thus computer-aided-engineering (CAE) is an effective tool for analyzing the complicated encapsulation process. [10]



10% fill 50% fill 90% fill

Figure 8: Insulation mold flow simulation pictures as an example (regular shaped I/O pads)

Mold flow simulation for lead frame packages can be used to optimize the lead frame design or internal package structure design as well as process parameters to reduce void defects and rejects without doing the actual molding experiments. Mold flow simulation of xGQFN 5x5mm was conducted to understand the melt front within the mold cavity and to check if the flow is well-balanced. Figure 8 above shows, simulation for insulation mold process showing well balanced melt front. Packing pressure, transfer profile, material and lead frame design were optimized and potential voids entrapment risk was mitigated.

Package Characterization

Thermal Analysis

With the routable technology which enables fully customizable lead frame design and full grid array I/O configurations, GQFN package offers alternative to 2-layers laminate base packages such as ball grid array (BGA) package at a lower cost and improved performance. Figure 9 below illustrates ball grid array (FBGA) comparing with GQFN.

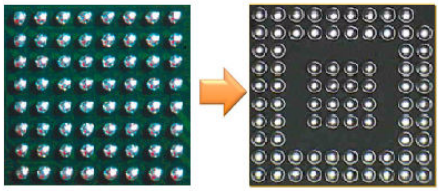
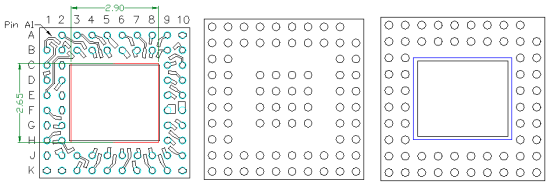


Figure 9: Conversion of laminate package, FBGA 5x5mm to GQFN 5x5mm (right)

GQFN offers the freedom of design to include a die attach paddle together with array of solder balls resulting in excellent thermal performance. Besides that, the central array copper pads and solder balls can be replaced with an exposed pad which further improves the thermal performance for high power usage. Figure 10 below shows the option available to convert two layers of laminates package BGA to lead frame based GQFN package.



Top View | Bottom View (Option 1) | Bottom View (Option 2)

Figure 10: xGQFN 5x5mm 79L Top and Bottom View

To evaluate the thermal performance of GQFN, thermal simulation and analyses were conducted on extra thin GQFN (both options) against FBGA using commercially available Computational Fluid Dynamics (CFD) software. For the purpose of comparative analysis, both packages are assumed to have the same die power, die size and die thickness. In CFD modelling method, the BGA substrate traces, GQFN lead frame traces and PCB traces are modelled as equivalent volume averaged layer with effective thermal conductivity. [11] Effective thermal conductivity is calculated using percentage of copper on top lead traces inclusive of die paddle for top layer and copper of terminal pads on the bottom layer. For a fair thermal comparison, both GQFN and BGA packages are assumed with the same percentage of copper on top and bottom layers. In this study xGQFN is used for evaluation hence the overmold thickness is at 0.25mm which encapsulates over top traces. The lead frame thickness is 0.1mm with the bottom half etch of 0.05mm encapsulated by insulation mold compound. For xGQFN option 1, there is a 3.0 x 2.5mm die paddle connected to 4x4 array of copper I/O pads, while in xGQFN option 2 the 4x4 array of copper I/O pads are replaced with 2.75 x 2.3mm exposed pad. The die size is fixed for all packages which is at 2.9 x 2.65mm. The package structure used in this study is shown in Figure 11 below.

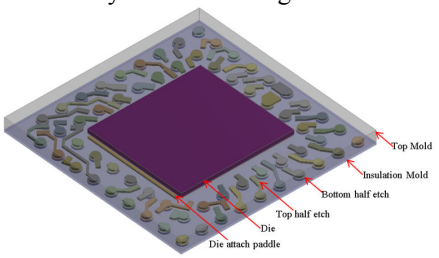


Figure 11: Package structure used in this study

The packages are simulated in test environments which complied with JEDEC standards JESD51-2A and JESD51-6 [12-13] to acquire Junction to Ambient thermal resistance (Theta JA) and Junction to Moving Air thermal resistance (Theta JMA) at air flow of 1m/s, 2m/s and 3m/s. Package materials used are according to UTAC's standard bill of materials for BGA and GQFN packages.

Table 2: Studies conducted for comparison

Leg#	Package design and assumptions	DA thermal conductivity
Leg 1	BGA 5x5mm(control)	1.5 W/mK
Leg 2	GQFN 5x5mm using DAF	0.3W/mK
Leg 3	GQFN 5x5mm using HT die attach	4W/mK
Leg 4	GQFN 5x5mm using HT die attach with epad	4W/mK
Leg 5	GQFN 5x5mm using HT die attach with epad and PCB vias	4W/mK

In this study, BGA package is used as a control package while GQFN is simulated with several different options namely, different die attach film material, high thermal die attach epoxy, package with exposed pad and exposed pad with PCB vias. This study is conducted with the purpose of presenting the potential thermal advantages using GQFN design instead of FBGA. Below are the results for thermal performance comparison:

Table 3: Thermal results

Thermal resistance	Air speed	Package Type				
		FBGA 5x5mm	xGQFN 5x5mm			
		Leg 1 (control)	Leg 2	Leg 3	Leg 4	Leg 5
Theta JA (°C/W)	0	61.4	53.7	46.3	43	30.9
Theta JMA (°C/W)	1	52.6	46.2	38.7	35.6	23.7
	2	51.0	44.7	37.3	34.2	22.5
	3	49.9	43.7	36.3	33.3	21.8

Package with lower thermal resistances will have better thermal performance. Based on this simulation GQFN packages are shown to have significant improved thermal performance compared to FBGA package across all designs. Performance

improvements for Theta JA at still air test environment are summarized below:

a) 12.5% improvement with xGQFN using DAF die attach (0.3W/mK)
b) 24.6% improvement with xGQFN using HT die attach (4W/mK)
c) 30% improvement with xGQFN with exposed pad
d) 49.7% improvement with xGQFN with exposed pad on PCB with thermal vias

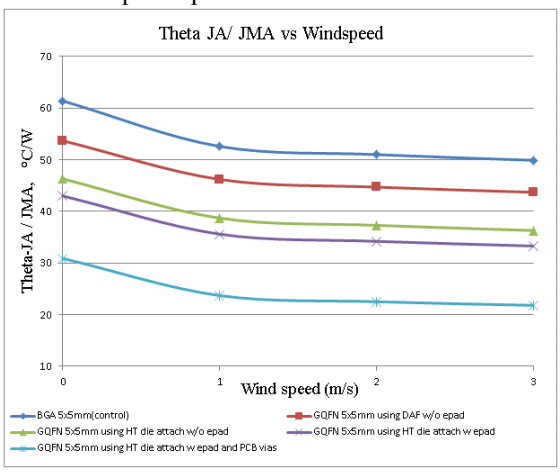


Figure 12: Thermal performance comparison between FBGA and xGQFN packages

Similar trend is observed for Theta JMA (1m/s, 2m/s and 3m/s) as shown in Figure 12 above. The comparison study shows that GQFN has better thermal performance than FBGA package and has the potential to improve thermal performance more than 40% using GQFN with exposed pad and PCB vias. GQFN using worse die attach film material still performs 12.5 % better than FBGA package which is mainly due to the heat spreading effect of die attach paddle that gives direct heat conduction from heat source to PCB via lead frame and solder, while in laminates based packages, the heat needs to be transferred from substrate layer-1 to layer-2 through limited substrate vias. As a conclusion, the thermal results showed that GQFN has superior thermal performance comparing to 2-layers FBGA at a much more competitive cost.

Electrical Analysis

Both FBGA5x5mm and xGQFN 5x5mm packages were simulated for electrical evaluation based on JEP126 standard. [14] ANSYS Q3D Extractor was used for parasitic extraction to obtain the RLC (resistance, inductance and capacitance) values to compare its package performance at low frequency while Advance Design System (ADS) is used for the S-Parameter Simulation to check each package performance at a higher frequency. For electrical modelling and assumptions, solder height is assumed at 0.1mm for GQFN and 0.17mm for FBGA, lead frame and substrate thickness is 0.1mm and 0.13mm respectively. Wire type for both packages is assumed 25um Au with the loop height of 0.1mm. Figure 13 below shows the extracted resistance, inductance and capacitance values for FBGA and GQFN. The higher parasitic value means lower performance. Based on the simulation results, there is no significant difference between the two packages. The electrical performance of GQFN package is as comparable to FBGA package at low frequency.

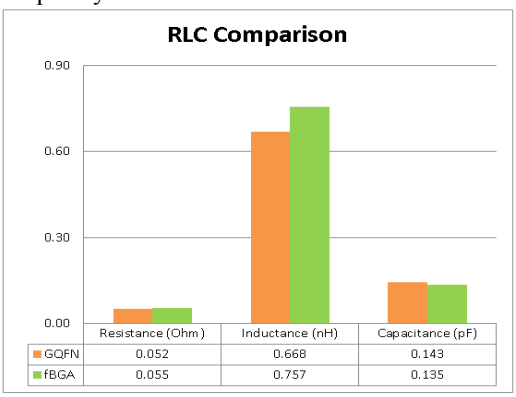


Figure 13: RLC comparison

For high frequency analysis, Scattering Parameter or S-Parameter is commonly used. The longest span of a signal was used to perform frequency sweep for each package. A good electrical performance of GQFN package can be seen up to 3.9 GHz, higher than the 2.85GHz of FBGA package. Limitation for return and insertion loss is -15 dB and -1dB respectively.

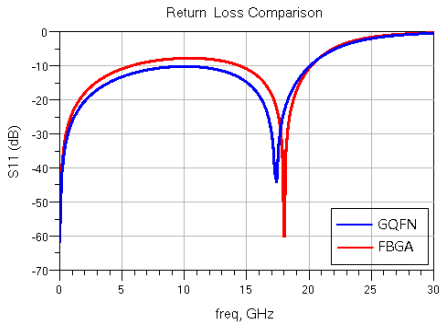


Figure 14: Return Loss

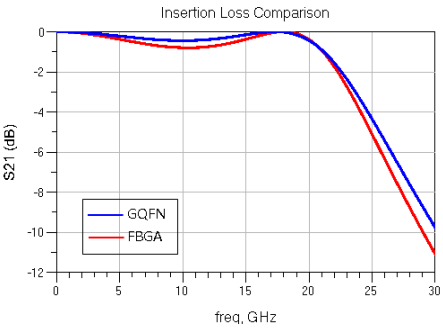


Figure 15: Insertion Loss

In conclusion, the electrical performance for both packages is comparable at low frequency. However, at higher frequency, GQFN package is better than FBGA package as FBGA package's electrical performance deteriorate 1GHz lower than GQFN package.

Board Level Reliability Test

Drop Test

The same package xGQFN 5x5x0.45mm with the die size of 2.9x2.6x0.1mm is subjected to board level reliability analysis. While the JEDEC standard requirement for drop test is minimum 30 drops, high expectation for shock resistance mobile devices requires packages to be compliance with harsher test standard which is up to 1000 drop cycles. Prior to the drop test experiment, xGQFN daisy chain packages were soldered on 132x77x1.0mm 8-layers board which was designed to form an integrated daisy-chain with packages through SMT process as per JESD22-B111. [15]

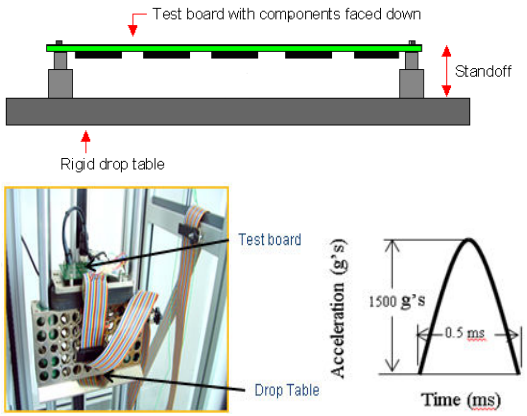


Figure 16: Drop test setup

Next, the board is mounted on the drop table with components faced down as shown in Figure 16 above. The test was conducted by controlling the drop height and free-fall dropping the board using drop table that corresponds to JEDEC Condition B (1500 Gs, 0.5 millisecond duration, half-sine pulse) The drop test results showed that the package xGQFN 5x5mm has excellent drop performance and passed 30 drops requirement. The first failure is recorded at 470 cycles with the characteristic life of 950 cycles. The characteristic life Weibull plot is shown in Figure 17 below.

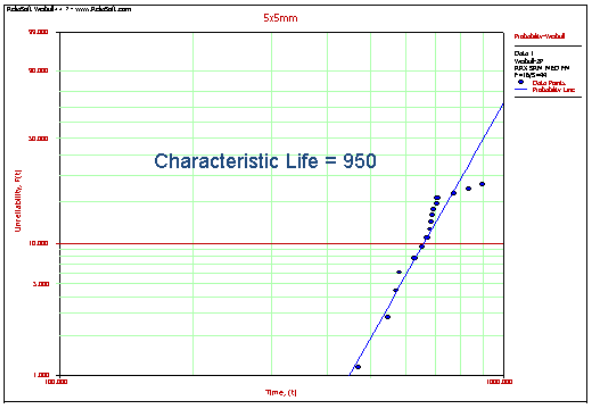


Figure 17: Weibull plot for drop test characteristic life

Temperature Cycle on Board Reliability Test

The board level reliability of semiconductor packages depends greatly on the state of stress, strain in solder interconnects, pad interfaces and nearby surrounding materials. During temperature cycle, stress and strain in the package fluctuates due to CTE mismatch which leads to the development of a looped stress-strain curve. As the cyclic stress prolongs, fatigue cracks eventually developed. [1] GQFN design has smaller package form factor with reduction of package size up to 60%, resulting in the increase of die-to-package ratio. Due to the increase in die-to-package ratio, there is a higher risk during board level thermal cycle reliability test. The die material silicon has low CTE which is the major source of CTE mismatch between package and PCB. Higher CTE mismatch induced higher solder joint stress resulting in earlier joint failure.

Twelve daisy chain xGQFN 5x5mm packages were mounted on 200x150mm 4-layer PCB and were subjected to accelerated life test to determine the second level reliability. Thermal cycling chamber was used for temperature cycling ranging between -40ºC to 125ºC with 15min dwell and 15min ramp, 1 cycle per hour according to IPC-9701A standard as in Figure 18 below. [16]

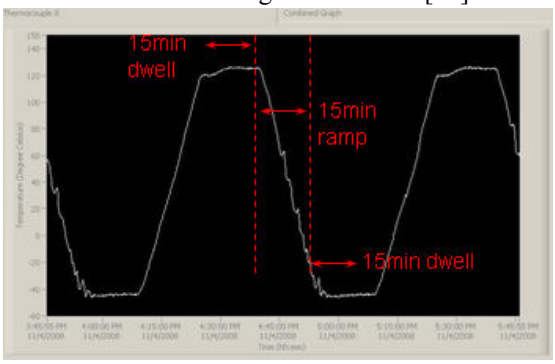


Figure 18: TCoB temperature cycle profile

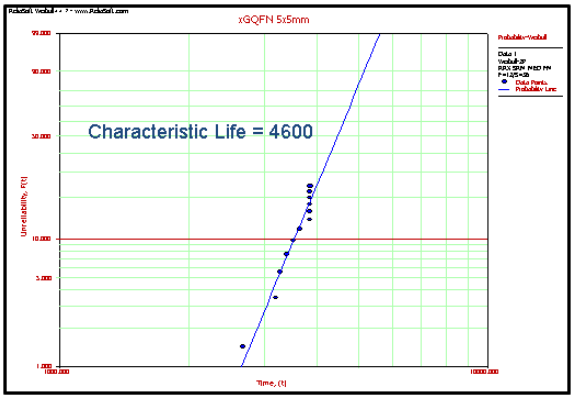


Figure 19: Weibull plot for TcOB characteristic life

The figure above shows the Weibull plot of xGQFN 5x5mm characteristic life which is the life cycles where 63.2% of the test components have failed. Despite the fact that the package's die-to-package ratio is 0.58, the package had excellent TCoB performance with first failure at 2,680 cycles and

characteristic life of 4,600 cycles. Failure analysis was performed by cross sectioning solder joint with scanning electron microscopy (SEM). Solder joint cracks occurs near package side at package to solder interface shown in Figure 20 below.

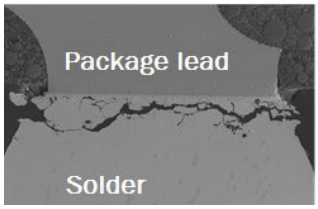


Figure 20: Cross sectional view of cracked solder joints

Package Level Reliability Test Results

Package level reliability test were conducted for JEDEC package or product qualification. Experimental moisture sensitivity level (MSL) test, accelerated moisture resistance – unbiased HAST (uHAST), temperature cycling (TC) and high temperature storage (HTS) were conducted for xGQFN 5x5mm 79L package.

Moisture sensitivity level test is to identify the classification level of non-hermetic package that are sensitive to moisture-induced stress so that devices can be properly packaged, stored and handled to avoid damage during typical industry multiple solder reflow. [17] uHAST is performed to evaluate the integrity of non-hermetic packages when exposed to high temperature and relative humidity environment. [18] Temperature cycling is to check ability of components and solder interconnects to withstand mechanical stresses induced by alternating high and low temperature extremes. [19] HTS is performed to check the effect of time and temperature under storage conditions. [20] The xGQFN 5x5mm package passed reliability test and showed good reliability data. The package reliability test results are summarized in Table 4 below:

Table 4: Package Reliability Test Results for xGQFN 5x5mm Package

1st Level Reliability			
Test	Standard	Conditions	xGQFN Package 5x5mm
Moisture Sensitivity Level Test	J-STD-020D.1, MSL1	168hrs, 85C/85% RH	Passed
Unbiased Temp/Humidity (uHAST)	JESD22-A118	130C/85% RH,96Hrs/192Hrs	96 Hrs-Passed 192Hrs-Passed
Temperature Cycle	JESD22-A104, TC Cond C	-65C to 150C, 500/1000cyc	500cyc-Passed 1000cyc-Passed
High Temperature Storage	JESD22-A103 & A113	150C, 500hrs/1000hrs	500Hrs-Passed 1000Hrs-Passed

Conclusions

The new package GQFN has been successfully developed and qualified. GQFN is an innovative product which enables design flexibility by allowing traces to be routed through etching process, providing higher I/O density, reduction of package size up to 60% and shorter wire length compared to QFN. The package can support stacked die, MCM, SiP using flip chip or wirebond interconnection. Development of an insulation mold process for GQFN enables production ramp up for high-volume manufacturing.

Thermal and electrical characterization indicated improvement in respective performance compared to FBGA. Both results highlighted excellent thermal and electrical characteristics with capability to handle high power and high-frequency requirements. Although the die-to-package ratio is high, board level reliability data for drop test and TCoB are presented with robust characteristic life and passed stringent requirements. In package level reliability test, the test vehicle exhibits good reliability data in accordance with JEDEC standards.

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