Thermal and Mechanical Analysis of Imaging Ball Grid Array Image Sensor Package

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Abstract

The growing demand of mobile phone, cameras and automotive pushes development of image sensor packaging in a trend of shrank form factor and more complex substrate design. To cater to the demand, the next generation image sensor package, Imaging Ball Grid Array (iBGA), was developed by UTAC. iBGA packages use organic substrates instead of ceramic carrier used in previous image sensor packages, for example, CLCC (Ceramic Leadless Chip Carrier) package. iBGA allows image sensor to become smaller, more advanced routings and alternative bill of materials to address specific material lead-times.

When a new packaging is developed, characterizations of the package are crucial. Finite element modeling and simulation approach is proven to be the most efficient and enable shorter time to market by elimination numerous engineering DOE and design-prototype-test cycles. Firstly, for any IC packaging, thermal performance is one of the factors needs to be considered as the new packaging type should not be so warm that will have negative impact on overall performance and reliability of the device. Secondly, as image sensor's essential part is a glass and glass is a brittle material, thermo-mechanical stress due to CTE miss-match to be resolved when developing the package.

In this paper, the characterization of UTAC image sensor package imaging ball grid array (iBGA) is studied. The structure and the packaging process of iBGA are illustrated. Thermal simulation is done using Computational Fluid Dynamic (CFD) simulation software to study heat dissipation and thermal performance under steady state condition with JEDEC standard. Moreover, mechanical simulation for warpage is conducted using Finite Element Analysis (FEA) simulation tool and correlated with Shadow Moiré measurement. Lastly, reliability examination is also done for iBGA. Studies will reveal the mechanical characteristics and thermal performance of the package in depth.

Introduction

Complementary metal-oxide semiconductor (CMOS) image sensors (CIS) started with lower image quality and higher noise in the past and were used for low cost products. [1]. With technology advancement of CMOS technology, CIS image quality is significantly improved making it alternative of CCD (charge-coupled device) image sensors. CIS nowadays are better than CCD in terms of frame rate, resolution, power consumption, noise performance and dynamic range. [2].

CIS has wide range of applications. From early of 21st Century, the boomed usage of mobile phone and inclusion of cameras in mobile phones created huge demand for image sensor. The pursuit of miniature shift application from CCD to CIS as CIS takes lesser space and consumes less power. Another main application of CIS is for automotive. CISs are used in car to provide drivers with surrounding views (Vision System) and to sense collisions (Sensing System). [3] The feature, higher dynamic range and higher frame rate, of CIS makes it a better option for application on automotive.

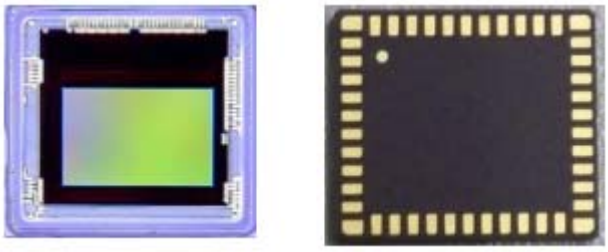
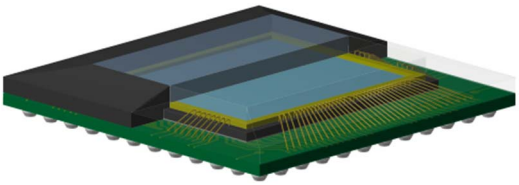
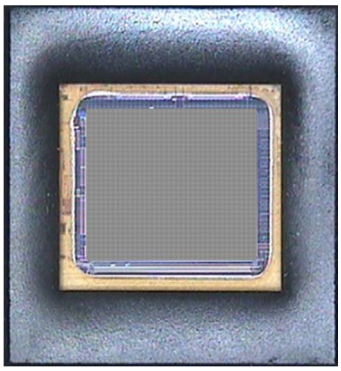


Fig. 1. CLCC Ceramic Package

CIS was first assembled with ceramic cavity. Dies are sitting inside cavity with walls surrounded and then covered by transparent glass. Because of ceramic material and side wall of ceramic cavity, ceramic based CIS package are costly and bigger in size. Ceramic substrates offer better performance in package warpage. In ceramic package, the mismatch of CTE (coefficient of thermal expansion) is minimized by the nature of ceramic material. [2] And the difference in thermal expansion across components in package is minimized during thermal cycles. Therefore, less package warpage and reduced stress. This improves both package level reliability, reduces chance of chip and glass cracking, and board level reliability, robust solder joint connection. The ceramic package also possesses good moisture protection and heat dissipation property. When the package is used in high temperature ambient like automotive application, better thermal dissipation eliminates heat build-up which is the cause of damage in silicon chip if the package temperature is higher than maximum allowable temperature 150°C. With advantages mentioned, there are also disadvantages of ceramic package. One of the downsides of ceramic package is design flexibility. Because of the complexity such as side wall plating and step cavity of ceramic substrate requires a more stringent design rule to follow than laminate substrate. Longer lead time for ceramic package is another disadvantage. [2] Competitive market and shorter product life cycles always demand shorter development time without sacrificing quality to be early in the market and gain more market shares. Ceramic substrate's longer lead time from sourcing suppliers to manufacturing and higher cost makes it less attractive compared to laminate substrate.



(a) 3D Model



(b) Package Top

Fig. 2. iBGA Organic Package

One of the alternatives for CIS ceramic substrate package is organic substrate package, iBGA. iBGA structure is similar to Ball Grid Array (BGA) packages. Die is sitting on top of organic substrate and interconnected by wire bond. Instead of covering die with encapsulant mold compound, iBGA is covered with glass and filled mold (Encapsulant). Compared to ceramic substrate, organic substrate is advantageous in lead time, cost and form factor optimization. [2] Manufacturing of organic substrate is shorter cycle time as a result of higher yields compared to ceramic substrate manufacturing. [4] In addition, higher yield brings down cost. Organic substrate also allows denser I/Os within limited form factor. [2] The routing design is also more flexible than ceramic substrate. However, using organic substrate in image sensor also brings in concerns. The first is organic substrate packages may have warpage issue if it is not designed carefully. Unlike low CTE ceramic material, organic substrate can have higher CTE mismatch with chips resulting in higher warpage. The second concern is package thermal dissipation. Since organic substrate thermal conductivity is lower than ceramic counterpart, higher thermal resistance is expected from iBGA without optimization. However, they can be addressed by structure and material enhancement during design stage.

The assembly process of iBGA package is shown in Fig. 3. iBGA assembly process starts from wafer back grind, which is required before assembly of the package in order to get a desired wafer thickness. After back grinding, dies are cut out from wafer during wafer sawing process. Chipping or delamination of wafer can be avoided by introducing a laser grooving process before sawing. The separated dies are then bonded onto substrate with dispensed epoxy at controlled heat and cured. To connect die to substrate, wire bond comes into play. During wire bonding process, heat and pressure are applied to form the connections. Glass is bonded on to the chip with glue dispense around the peripheral forming air cavity window at the center. The glass window area allows external light projection on active image pixel array of the sensor. Then molding process proceeds with dam and fill liquid encapsulation method following by laser marking. Thereafter, ball mount and reflow process take place at high temperature. Finally, after strips cool down from reflow temperature, singulation is done to form individual iBGA packages.

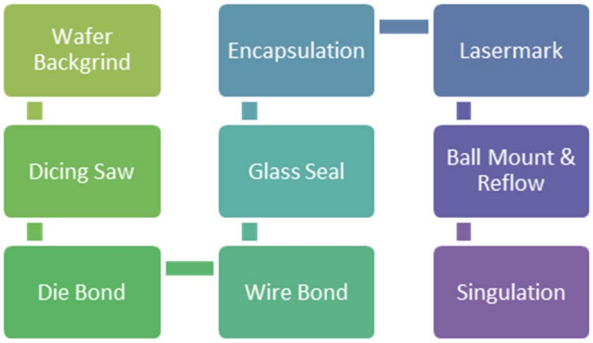


Fig. 3. iBGA Assembly Process Flow

The package structure of CLCC and iBGA are shown in Fig. 4 and 5 below. In the figures, encapsulant, glass, die and substrate stack-up are illustrated clearly.

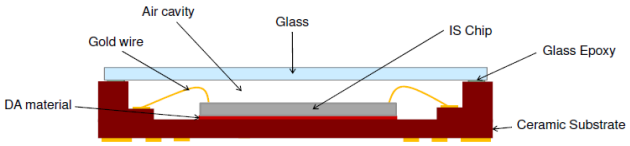


Fig. 4. CLCC Package Cross Section View

In the CLCC package, a 7x5 mm chip is placed on and surrounded by ceramic substrate. Glass with thickness of 0.5mm is placed on top of ceramic substrate that is 1.3mm in thickness and chip is enclosed. On the other hand, for iBGA package, the chip is sitting on a 2 layers organic substrate of 0.28mm thick. Chip is connected to substrate by wire bonds. Both chip and glass side are surrounded by encapsulant material.

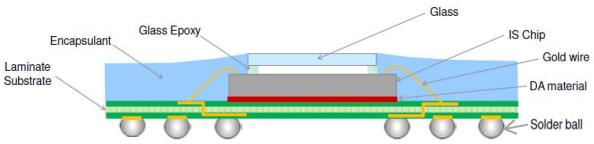


Fig. 5. iBGA Package Cross Section View

Thermal Analysis

Heat is transferred in three ways; conduction, convection and radiation. Conduction happens when solid objects are in contact, the temperature difference between bodies creates potential for heat to flow from higher temperature bodies to lower temperature ones. In the iBGA package, for example,

heat source is the die or image sensor chip, which has the highest temperature in the system during operation. Die attach (DA) material, encapsulant and glass's epoxy are in direct contact with die and heat is transferred from die to them through conduction. As they are also in contact with other material in the package, paths of heat conduction are formed as shown in schematic drawing below. To top side is die→ glass glue→ encapsulant + glass. Path to the bottom side is die→die attach → substrate→solder balls→PCB. And die→ encapsulant at the side.

Convection happens at the interface of fluid and solid objects. When the fluid flows, heat is transferred from high temperature body to the lower one. In this study, ambient air is the fluid with lower temperature and iBGA package is the solid object with higher temperature. Convection happens mainly at top and side of package and PCB. Radiation is the type of heat transfer that requires no contact. Heat is transmitted out from hot body. In the study, package and PCB emit heat to the ambient. The radiation path is similar to convection heat path as illustrated in Fig. 6. Blue arrow represents conduction heat flow and orange arrow indicates convection and radiation heat flow.

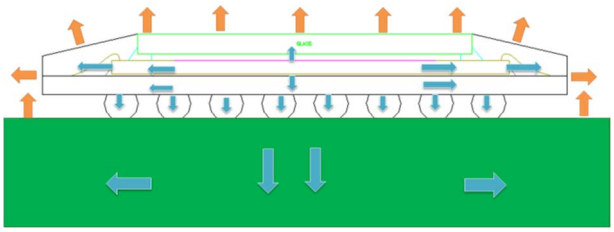


Fig. 6. Heat Flow Path

The most common measure of package's thermal characteristics is thermal resistance theta Junction-to-Ambient ($R_{\theta_{JA}}$), which describes, as the name suggests, thermal resistance from die junction to ambient. The formula of $R_{\theta_{JA}}$ is

$$R_{\theta_{JA}} = \frac{T_J - T_a}{P}$$

Where T_J is die junction temperature, T_a is ambient temperature and P is power dissipation of the die.

Table 1. Ceramic Package Options [5]

Package	CLGA198	CLGA104	CLGA102	CLGA074	CLCC046	CLCC042	CLCC040	CLCC038
Package Size (mm)	21.9x27.0	12x14.5	11.3x13.3	10.2x11.6	8.3x9.4	8.3x9.4	10.0x12.0	8.3x9.4
Pin count	198	104	102	74	46	42	40	38
Substrate Thickness (mm)	1.95	1.65	1.3	1.3	1.0	1.0	1.0	1.0
Glass Thickness (mm)	0.7	0.5	0.5	0.3	0.5	0.3	0.5	0.5
Package Height (mm)	2.65	2.15	1.8	1.6	1.5	1.3	1.5	1.5
Seal width (mm)	1.33	1.125	0.78	0.6	0.4	0.4	0.4	0.4
Max Chip size (mm)	17.2x22.1	7.5x9.1	7.9x9.1	7.4x8.3	6.9x7.8	5.9x7.6	7.0x9.9	5.9x7.6
Chip Thickness (mm)	0.65	0.65	0.3	0.3	0.2	0.3	0.3	0.3
D0 (Image to bottom PKG)	1.25mm	1.25mm	0.9mm	0.9mm	0.8mm	0.6mm	0.6mm	0.6mm
D1 (Image to glass top)	1.4mm	0.9mm	0.9mm	0.7mm	0.7mm	0.7mm	0.9mm	0.9mm
Wire type	Au	Au	Au	Au	Au	Au	Au	Au
Wire diameter (um)	17.5	17.5	17.5	17.5	17.5	22.5	22.5	22.5
Number of Wires	328	103	121	104	67	41	39	37

Above Table 1. shows the available size of ceramic packages. [5] To fit in a CIS chip of 7 x 5mm and also to minimize the package size, 8.3 x 9.4mm CLCC package is selected. Because iBGA is more flexible in body size and routing, the same chip can fit in smaller 8 x 8mm package.

For both iBGA 8 x 8mm and CLCC 8.3 x 9.4mm packages, thermal simulations are conducted using computational fluid dynamics (CFD) software FloTHERM with JEDEC standards set up. The main thermal performance indicator, i.e. Junction to ambient thermal resistance Theta JA is simulated under the test environment of natural convection as per JEDEC 51-2A. [6] as shown in Fig.7 below. In an enclosed air box 305 x 305 x305 mm, the package is soldered to JEDEC 2s2p PCB with dimension 101.5 x114.5 x1.6mm according to JEDEC 51-9. [7] PCB is connected to test fixture by a socket.

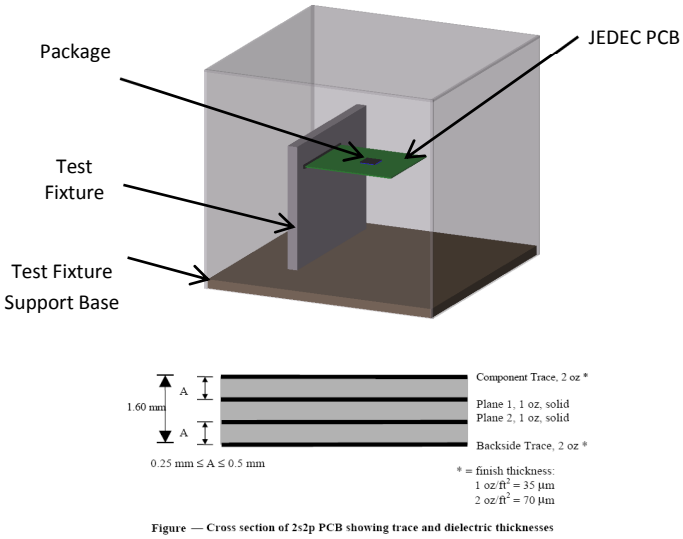


Fig. 7. Still Air Test Box

Table 2. Thermal conductivity of material

W/mK	CLCC	iBGA
Ceramic	14	-
Organic Substrate Core	-	0.8
Trace	198	385
Die attach Epoxy	0.4	0.4
Encapsulation	-	0.5
Si Die	117.5-0.42*(T-100)	117.5-0.42*(T-100)

Table 3. Thermal Simulation Result

Package Type	Thermal Resistance Theta JA (°C/W)
CLCC	33.2 (Baseline)
iBGA	33.4 (↑0.57%)

With material properties showing in Table 2, the simulation results (in Table 3) show that iBGA 8 x 8mm can achieve comparable thermal performance as the CLCC 8.3 x

9.4mm and the difference is less than 1%. Fig. 8. and Fig. 9. illustrate heat dissipation for iBGA and CLCC packages on JEDEC PCB. In iBGA package, more heat dissipation can be observed at the top glass surface which helps to cool the chip junction temperature.

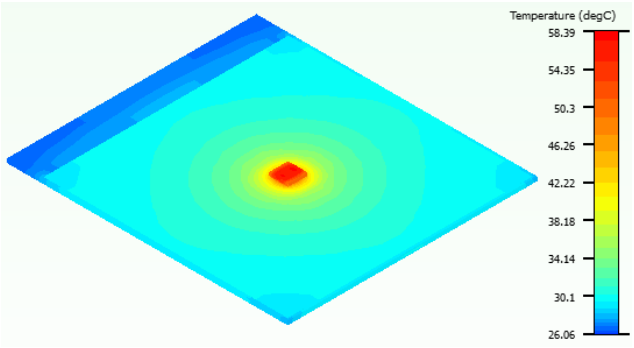


Fig. 8. iBGA Heat Distribution

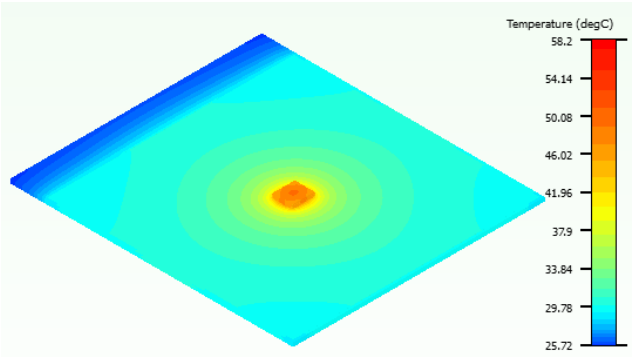
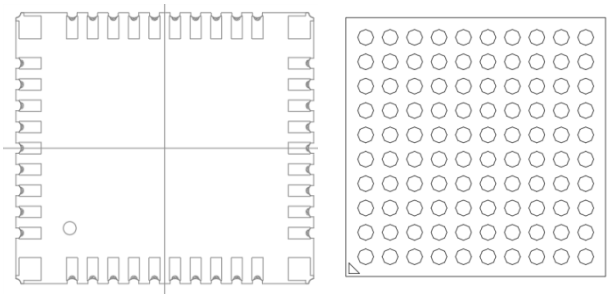


Fig. 9. CLCC Heat Distribution



CLCC 8.3 x 9.4mm iBGA 8x8mm

Fig. 10. CLCC & iBGA Package Outline (bottom view)

The Package Outline Drawing (POD) of CLCC and iBGA is shown in Fig.10. It can be seen that full array of ball enables iBGA to accommodate thermal balls at the center of the package bottom while CLCC only has peripheral pins. This feature makes it possible to connect PCB thermal vias for iBGA but not CLCC. Therefore, PCB thermal vias are included in study below. Vias help to deliver heat from package bottom to deeper layers of PCB and spread out further across PCB. The bigger surface area of PCB compared to the package facilitates faster convection heat transfer to the surroundings. The table below shows simulation result of packages with inclusion of PCB thermal vias for iBGA package. It is clearly showed that the selected iBGA with PCB vias will have better performance over CLCC package.

Table 4. Thermal Simulation Result 2

Package Type	Thermal Resistance Theta JA (°C/W)
CLCC	33.2 (Baseline)
iBGA	33.4 (↑0.57%)
iBGA with PCB Thermal Vias	28.1(↓15.5%)

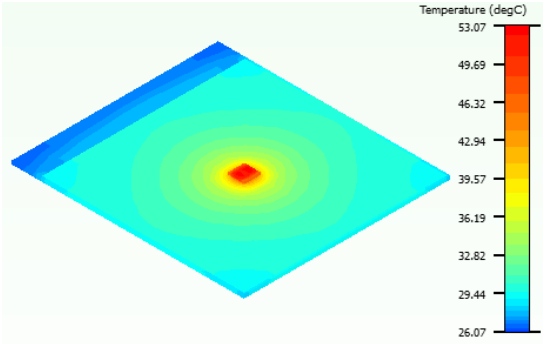


Fig. 11. iBGA with PCB thermal Vias Heat Distribution

Mechanical Analysis

The package warpage induced by coefficient of thermal expansion (CTE) mismatch between the various packaging materials during thermal cycling (TC) is one of the major thermo-mechanical reliability concerns in IC packaging. The occurrence of excessive unit warpage can lead to misalignment of parts and a variety of operational failures such as chip and glass cracking, delamination and solder joints failures. iBGA package have been found to be more susceptible to package warpage compare to ceramic counter parts. Therefore, the warpage requirements must be satisfied and package design, structure and material optimization is a must.

Finite element analysis (FEA) is performed on iBGA package to characterize package warpage and thermo-mechanical stress focus on glass and image sensor (chip) since they are at high risk of possible cracks during thermal cycling. Full 3D model, Fig.12., is constructed with glass, encapsulant, sensor, glue coverage and substrate details. Meshing is controlled carefully such that element nodes are match at the interface especially between the glass and encapsulant where the high stress is expected. Assuming stress free temperature is 165°C, the package level warpage and maximum principal stress are studied at room temperature 25°C. All materials properties are assumed

linear elastic.

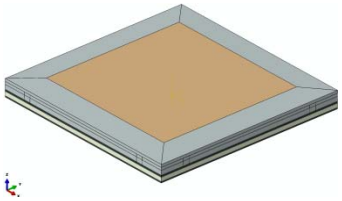
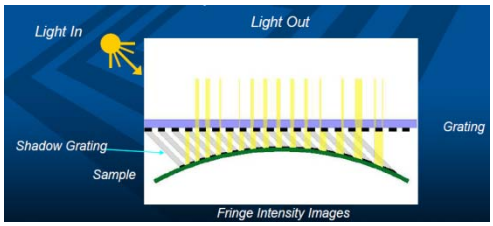


Fig. 12. 3D FEA Model

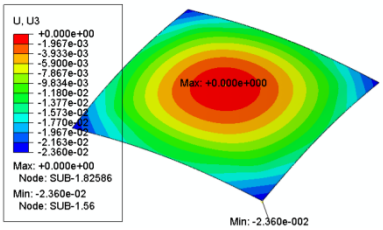
Actual warpage measurement based on Shadow moiré technique was done to validate FEA simulation predictions. Shadow moiré uses geometric interference between a reference grating and its shadow on a sample to measure relative vertical displacement at each pixel position in the resulting interference pattern image. It requires a Ronchi-ruled grating, a white line light source at approximately 45 degrees to the grating, and a camera perpendicular to the grating. The principle of Shadow moiré is illustrated in the figure below. [8].



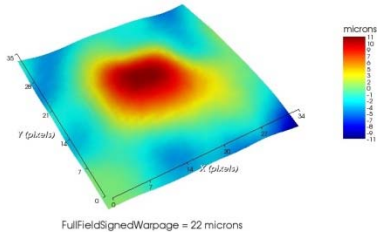
Source: akrometrix [8]

Fig. 13. Principle of Shadow Moiré

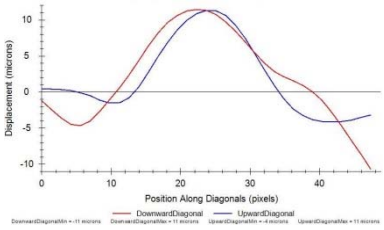
FEA simulation prediction of package warpage 23.6um is well correlated with Shadow moiré warpage measurement of 22 um as shown in below figures.



(a). Simulation prediction (warpage 23.6um)



(b). Warpage measurement (Full field warpage 22um)



(c). Warpage measurement (diagonal)

Fig. 14. Package Warpage Comparisons

Repeated bending of the package during thermal cycling can cause package cracks if the warpage is not properly controlled. Fig. 15. shows simulation stress distribution and section view of the actual glass cracks. Simulation results show that high stress region at the center of the glass lid where actual glass cracks occurred.

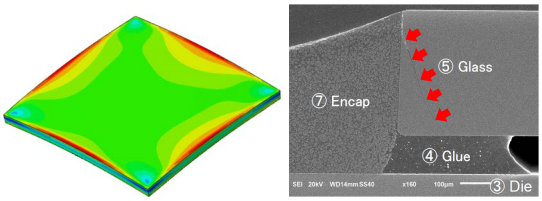


Fig. 15. Stress Distribution and Glass cracks

To mitigate glass stress, Design of Experiments (DOEs) including various glass material, glass sizes, glass thicknesses, metal layers of laminate substrate, die thicknesses, Encapsulant material, Encapsulant heights and with/without encapsulant were studied focus on cracks region. Fig. 16 shows one of the DOE legs where different glass sizes impact on glass stress were studied. From simulation results, bigger glass reduced the glass stress effectively. The maximum glass stress decreased 16% from 149MPa to 125MPa when the glass size increased from 6.2 x 5.2mm to 6.6x7.2mm. Table 5 is the summary affecting the factors affecting the stress on glass.

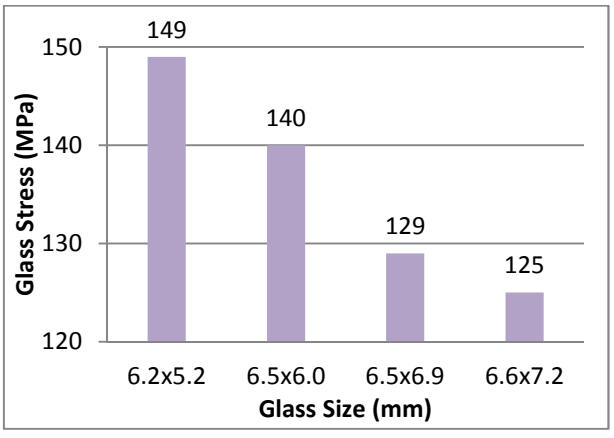


Fig. 16. Glass Stress vs Glass Size

Table 5. Design and material impact on glass stress

Leg No	Die thickness	Glass size	Glass thickness	Encapsulant material	Max stress
1	+	+	-	A	Ref
2	+	-	-	A	↑
3	+	--	-	A	↑↑
4	+	++	-	A	↓
5	+	+	+	A	-
6	-	+	+	A	↓
7	+	+	-	B	↓↓

Fig. 17. shows die stress comparison with respect to glass seal thickness. Die stress is lowered by 58 MPa by increasing glass seal thickness from 0.09mm to 0.125mm. Stress distribution is illustrated in Fig.18.

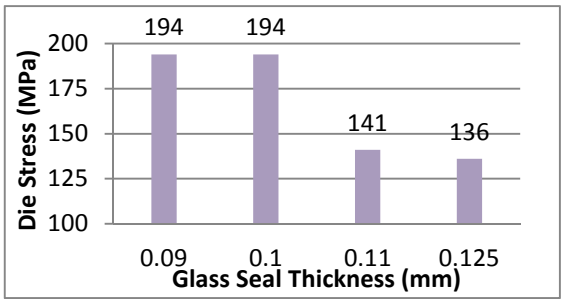
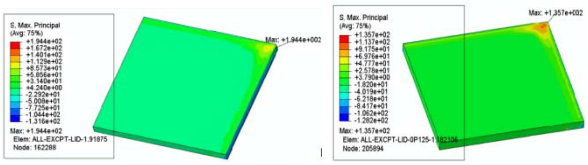


Fig. 17. Die Stress vs Glass Seal Thickness



Glass seal thickness = 0.09 mm
Die max stress = 194 Mpa

Glass seal thickness = 0.125 mm
Die max stress = 136 Mpa

Fig. 18. Die Stress w/ Glass Seal Thickness of 0.09 & 0.125 mm

Reliability Results

The package reliability test results iBGA package is summarized in Table 5 below. iBGA package is meeting AEC-Q100 Grade 2 reliability requirements.

Table 6. Package's Reliability test result

Test Condition	Time Zero	1000cyc / 1000hrs
Preconditioning MSL3 + Reflow 260°C	PASS	PASS
TC (-55°C / +125°C)	PASS	PASS
THB (85°C / 85% RH)	PASS	PASS
HTSL (125°C)	PASS	PASS

Conclusion

iBGA package technology provides an alternative solution to image sensor packaging with lower cost, faster lead time and design flexibility. iBGA also shows comparable thermal performance while providing smaller foot print compared to CLCC. iBGA's capability to cater full ball array in 8 x 8mm foot print enables the possibility to include center thermal balls which can be connected to PCB thermal vias. This allows iBGA package to offer thermal enhancement option that assist thermal dissipation better than CLCC. Lower thermo-mechanical stress and better reliability of iBGA package can be achieved by fine tuning of package design and material with proven results of iBGA meeting stringent AEC-Q100 G2 reliability.

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